

Formal support for Untimed SystemC Specifications: Application to High-Level Synthesis



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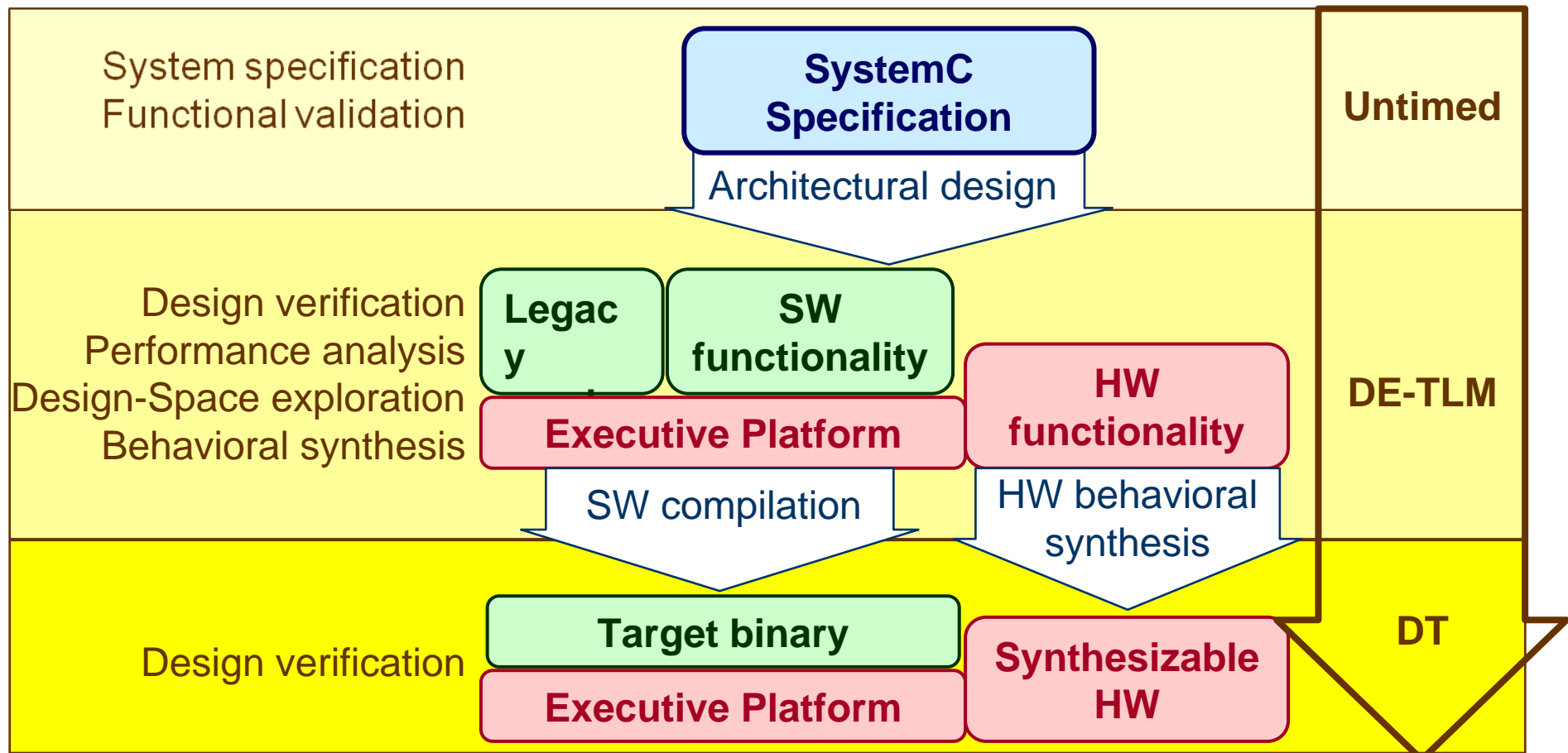


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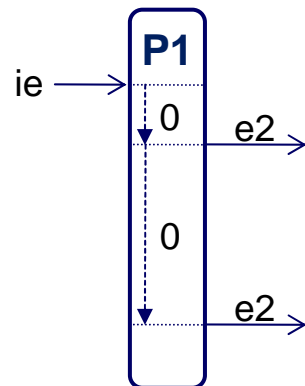
Motivation

- SystemC applications



Motivation

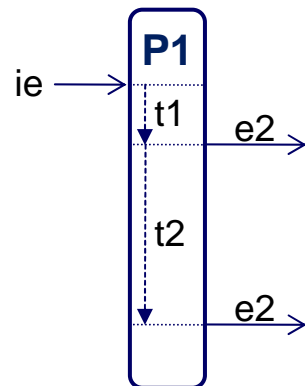
- Timing transformations
 - Source of design errors
 - Classical problem in concurrent programming
 - Not enough addressed in system (HW/SW) design



System simulation

Motivation

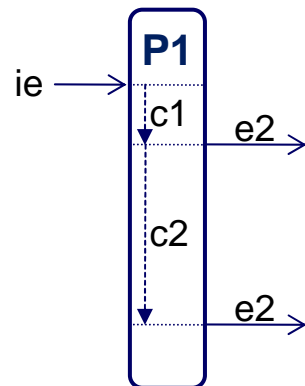
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TLM simulation

Motivation

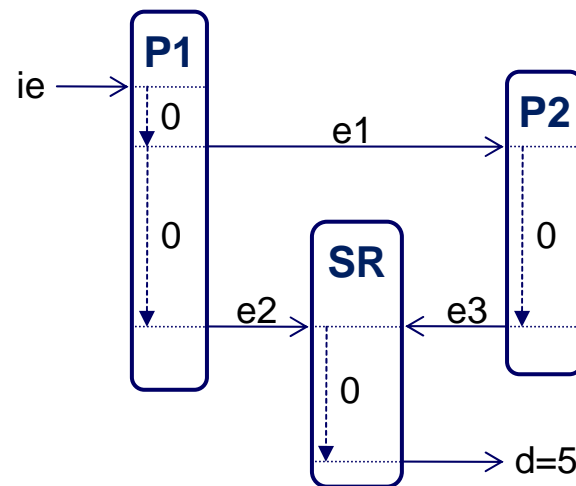
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Cycle simulation

Motivation

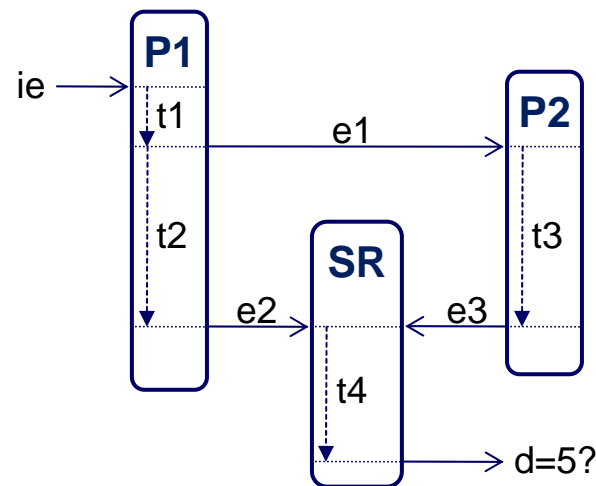
- Timing transformations
 - Source of design errors
 - Classical problem in concurrent programming
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System simulation

Motivation

- Timing transformations
 - Source of design errors
 - Classical problem in concurrent programming
 - Not enough addressed in SystemC (HW/SW) design

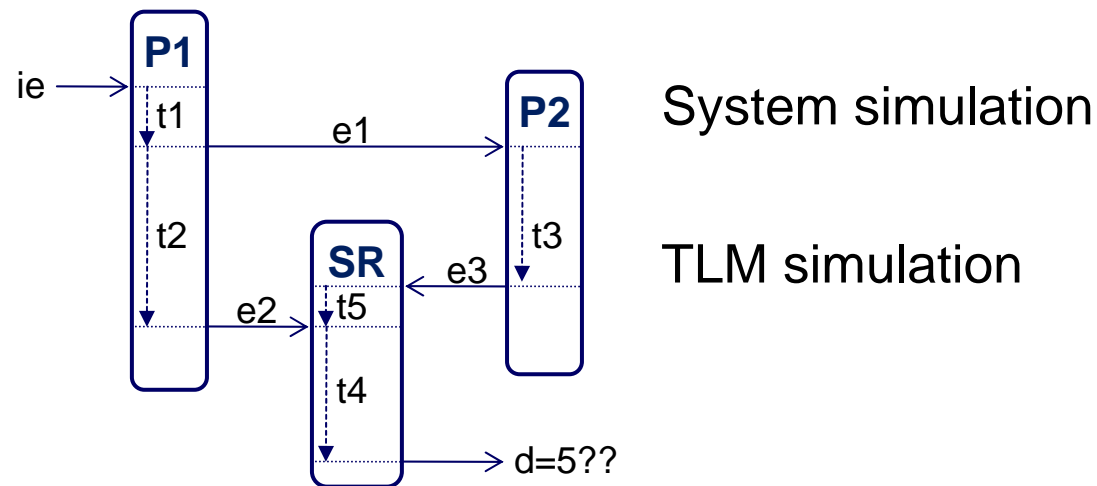


System simulation

TLM simulation

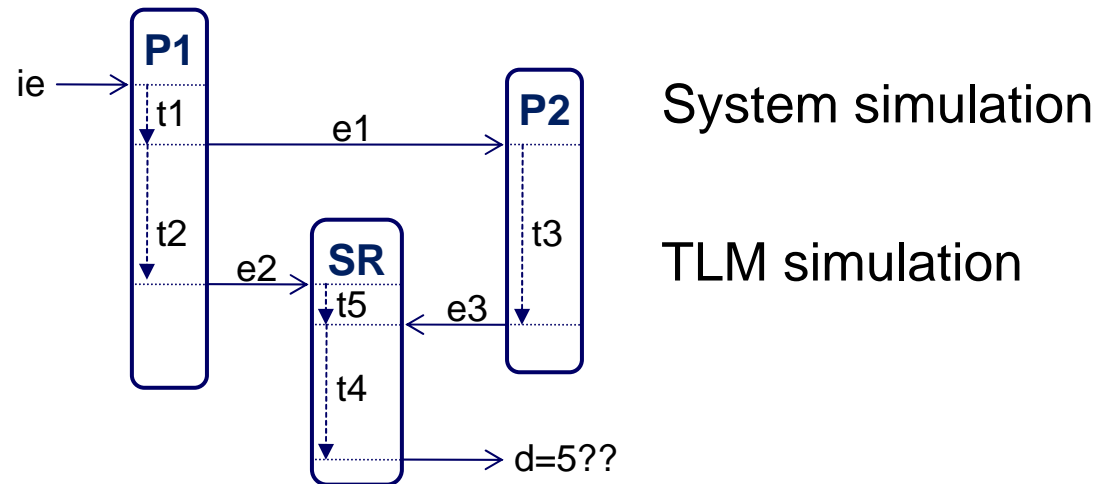
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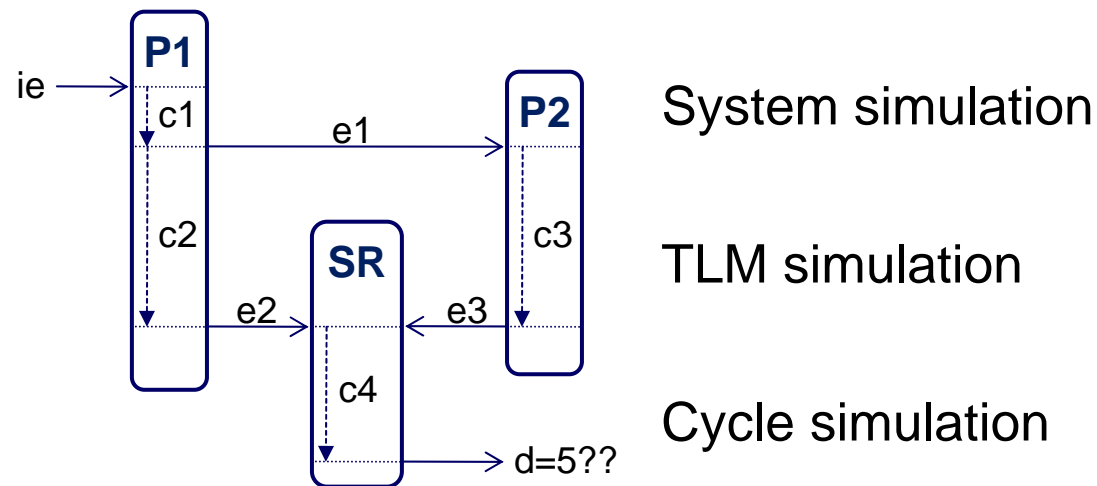
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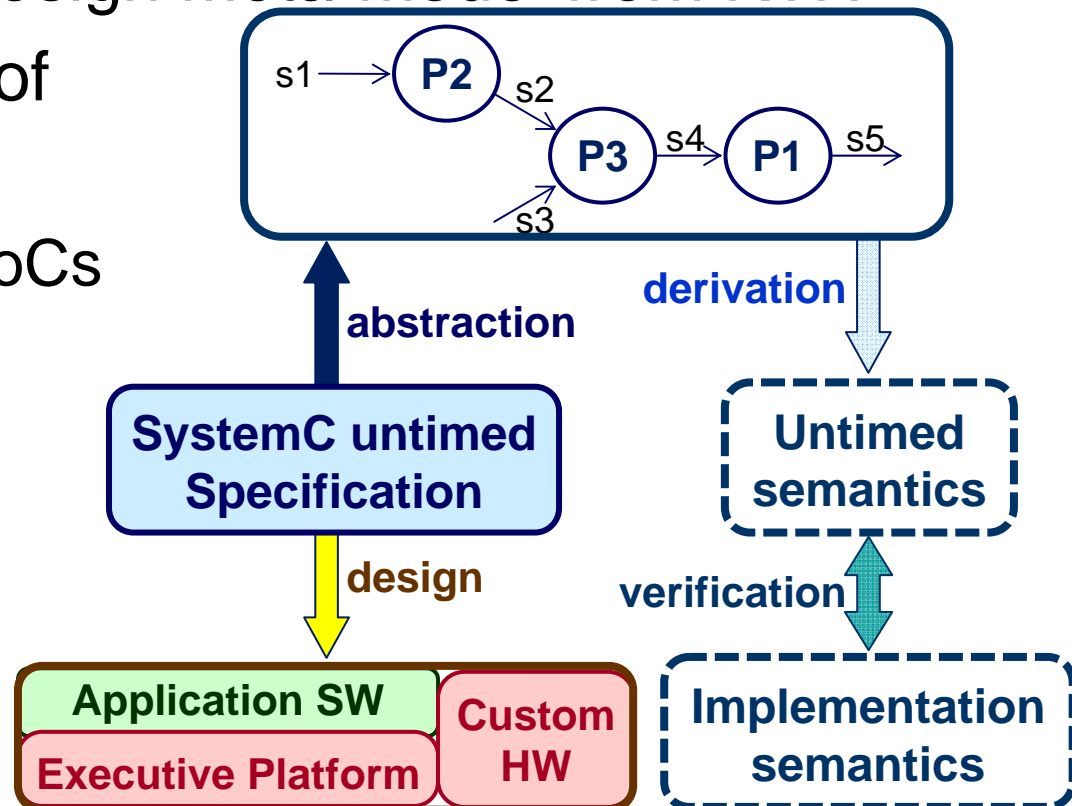


Motivation

- Need for formal support
 - SystemC-based design
 - Timing transformations
 - From Untimed Specifications
 - Down to TLM and Cycle-accurate implementations

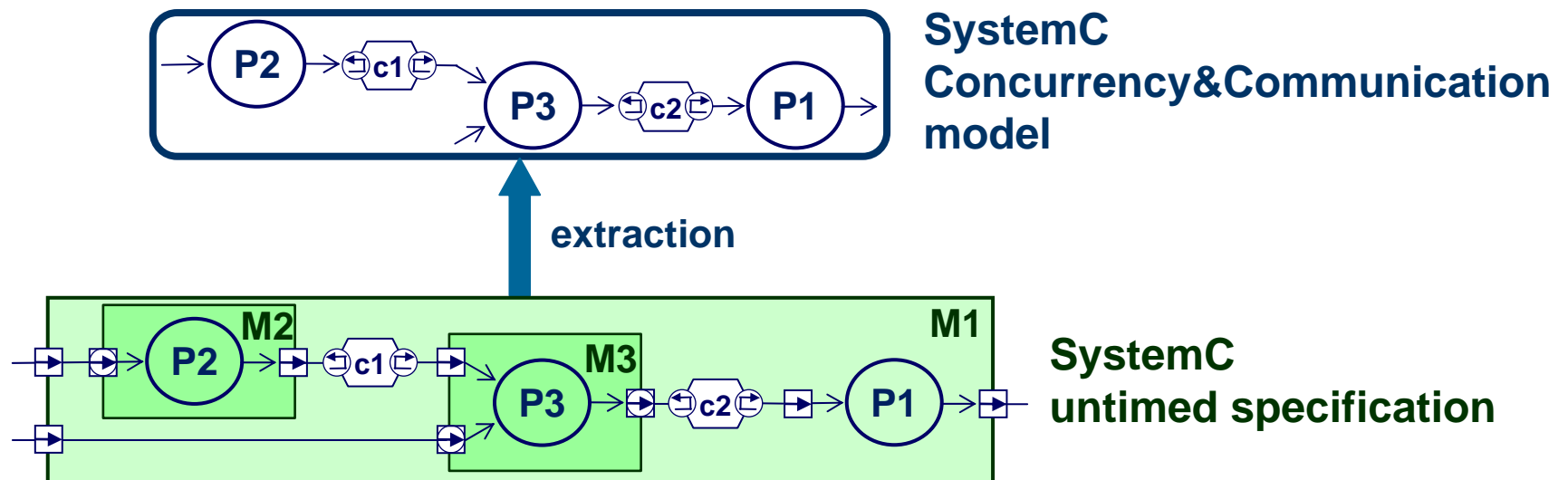
Introduction

- ForSyDe
 - Formal System Design meta-model from KTH
 - Formal definition of
 - Untimed MoCs
 - Synchronous MoCs
 - Timed MoCs



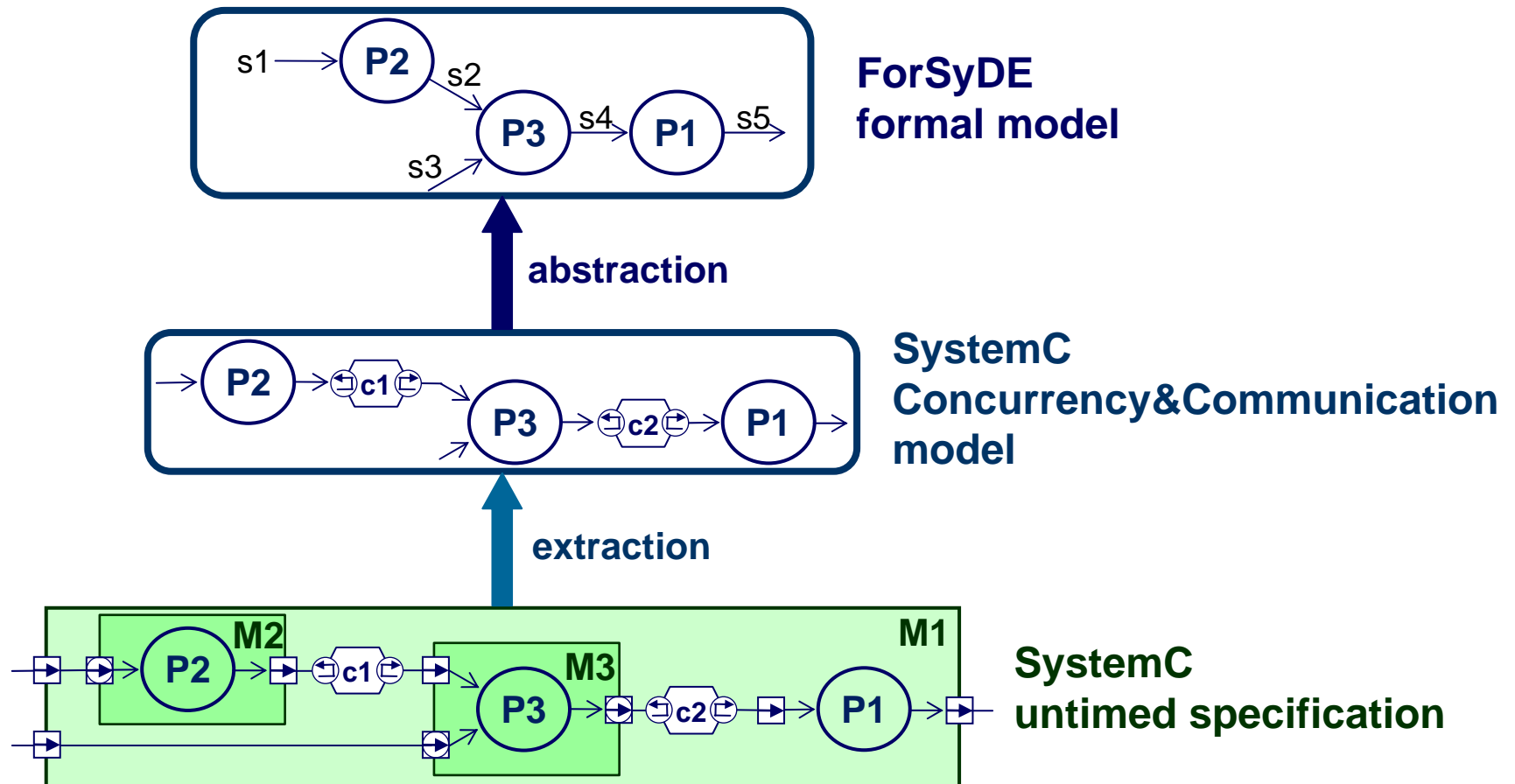
Formal Framework

- Extraction of the SystemC C&C model
 - Removal of hierarchical facilities
 - Flat model of communicating concurrent processes



Formal Framework

- Abstraction of the formal model



Formal Framework: Simple Example

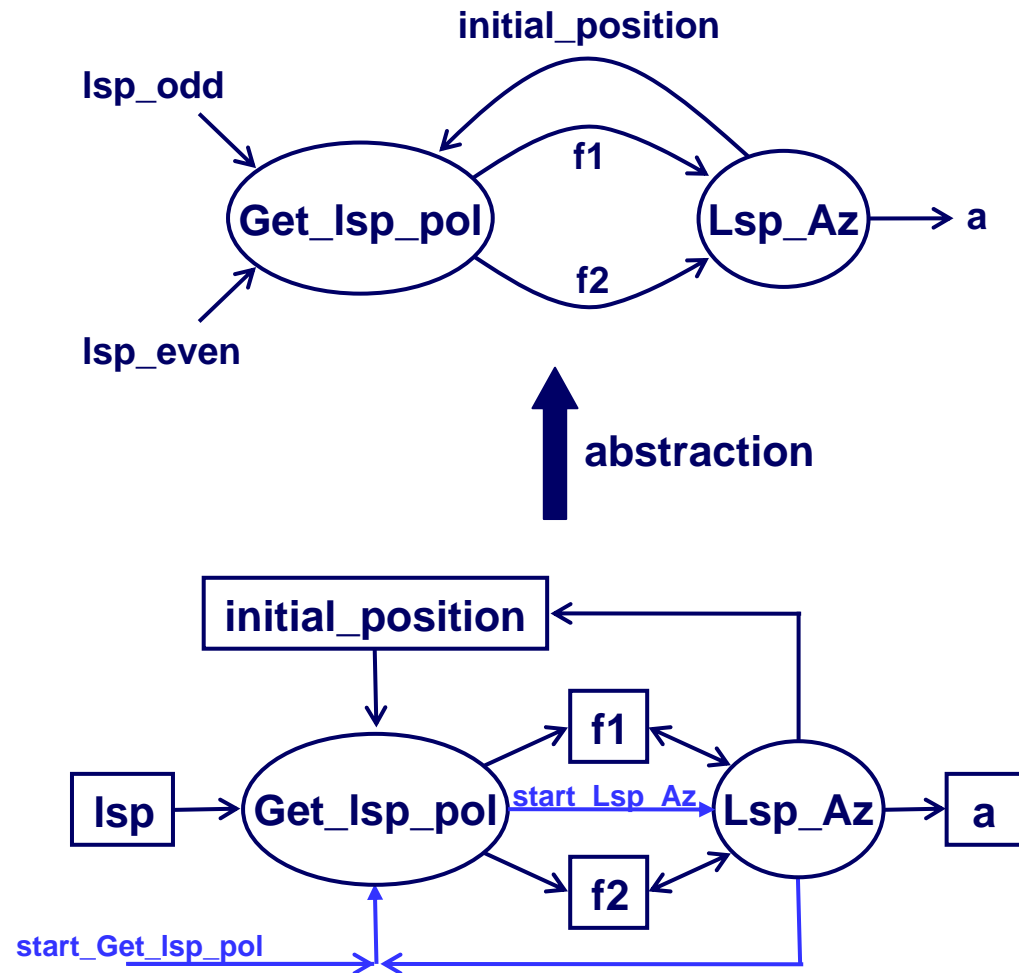
```

SC_MODULE(Simple_Example) {
  . Port declarations
  . Channel/submodule instances
  Word16 lsp[10], a[11];
  int initial_position=0;
  Word32 f1[6], f2[6];
  sc_event start_Get_Lsp_pol; start_Lsp_Az;
  SC_CTOR(Simple_Example) {
    . Connectivity
    SC_THREAD(Get_Lsp_pol);
    SC_THREAD(Lsp_Az); }

  void Get_Lsp_pol() {
    while (true) {
      wait(start_Get_Lsp_pol);
      . Get_Lsp_pol computes f1 from the odd positions
      . or f2 from the even positions of 'lsp' depending
      . on the value of 'initial_position'
      notify (start_Lsp_Az); }
  }

  void Lsp_Az() {
    while (true) {
      wait(start_Lsp_Az);
      initial_position = 1;
      notify(start_Get_Lsp_pol);
      for (i=5;i>0;i--) f1[i]=L_add(f1[i],f1[i-1]);
      wait(start_Lsp_Az);
      initial_position = 0;
      for (i=5;i>0;i--) f2[i]=L_sub(f2[i],f2[i-1]);
      . a is computed from f1 and f2
    }
  }
}

```



Formal Framework: Simple Example

```
SC_MODULE(Simple_Example) {
  . Port declarations
  . Channel/submodule instances
  Word16 lsp[10], a[11];
  int initial_position=0;
  Word32 f1[6], f2[6];
  sc_event start_Get_Lsp_pol; start_Lsp_Az;
  SC_CTOR(Simple_Example) {
    . Connectivity
    SC_THREAD(Get_Lsp_pol);
    SC_THREAD(Lsp_Az); }
}
```

```
void Get_Lsp_pol() {
  while (true) {
    wait(start_Get_Lsp_pol);
    . Get_Lsp_pol computes f1 from the odd positions
    . or f2 from the even positions of 'lsp' depending
    . on the value of 'initial_position'
    notify (start_Lsp_Az); }
}
```

```
void Lsp_Az() {
  while (true) {
    wait(start_Lsp_Az);
    initial_position = 1;
    notify(start_Get_Lsp_pol);
    for (i=5;i>0;i--) f1[i]=L_add(f1[i],f1[i-1]);
    wait(start_Lsp_Az);
    initial_position = 0;
    for (i=5;i>0;i--) f2[i]=L_sub(f2[i],f2[i-1]);
    . a is computed from f1 and f2
  }
}
```

```
Get_Lsp_pol = mapU(1, vlsp_odd, vlsp_even, f, f)
```

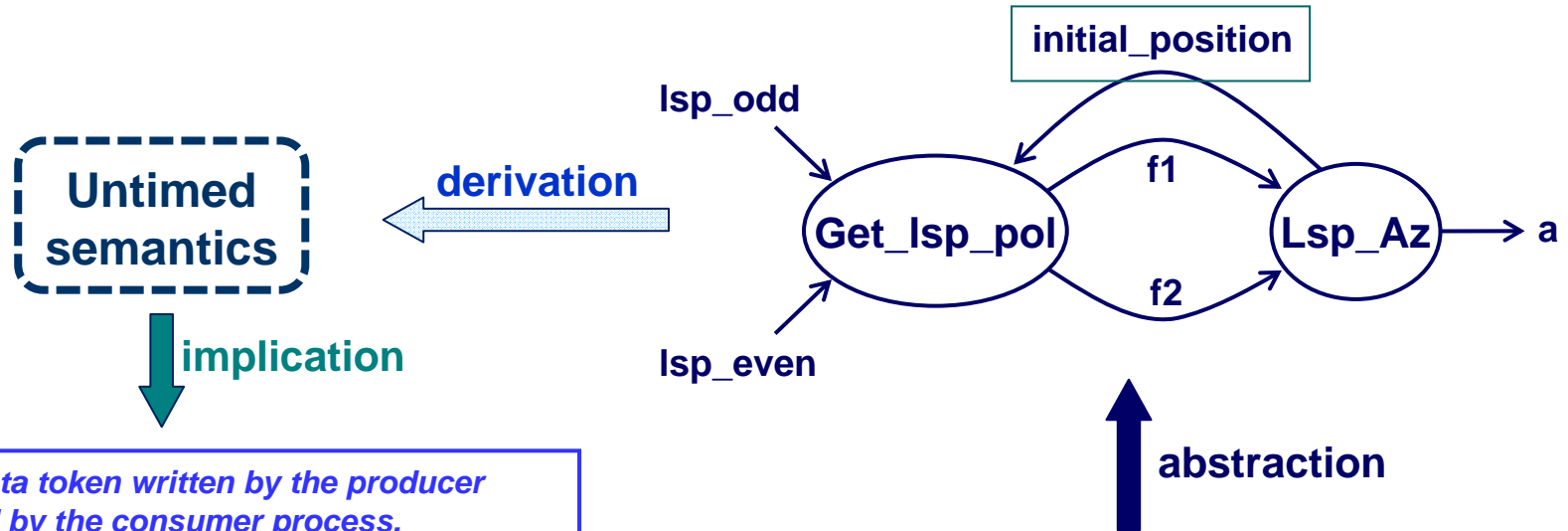
```
Get_Lsp_pol(initial_position, lsp_odd, lsp_even) = <<f1><f2>>
//an 'initial_position' value is always taken
 $\pi(v_{\text{initial\_position}}, \text{initial\_position}) = \langle \text{initial\_position}_i \rangle$ 
 $v_{\text{initial\_position}}(i) = 1$ 
If (initial_positioni = 0) then
  f1i = f(lsp_oddi)
  //five 'lsp_odd' data are taken but no 'lsp_even'
   $\pi(v_{\text{lsp\_odd}}, \text{lsp\_odd}) = \langle \text{lsp\_odd}_i \rangle$ 
  vlsp_odd(i) = 5
   $\pi(v_{\text{lsp\_even}}, \text{lsp\_even}) = \langle \text{lsp\_even}_i \rangle$ 
  vlsp_even(i) = 0
  //six 'f1' data are generated but no 'f2'
   $\pi(v_{f1}, f1) = \langle f1_i \rangle$ 
  vf1(i) = 6
   $\pi(v_{f2}, f2) = \langle f2_i \rangle$ 
  vf2(i) = 0
else
  f2i = f(lsp_eveni)
  //five 'lsp_even' data are taken but no 'lsp_odd'
   $\pi(v_{\text{lsp\_odd}}, \text{lsp\_odd}) = \langle \text{lsp\_odd}_i \rangle$ 
  vlsp_odd(i) = 0
   $\pi(v_{\text{lsp\_even}}, \text{lsp\_even}) = \langle \text{lsp\_even}_i \rangle$ 
  vlsp_even(i) = 5
  //six 'f2' data are generated but no 'f1'
   $\pi(v_{f1}, f1) = \langle f1_i \rangle$ 
  vf1(i) = 0
   $\pi(v_{f2}, f2) = \langle f2_i \rangle$ 
  vf2(i) = 6
```

Formal Framework: Simple Example

```
SC_MODULE(Simple_Example) {  
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    SC_THREAD(Get_Lsp_pol);  
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  void Get_Lsp_pol() {  
    while (true) {  
      wait(start_Get_Lsp_pol);  
      . Get_Lsp_pol computes f1 from the odd positions  
      . or f2 from the even positions of 'lsp' depending  
      . on the value of 'initial_position'  
      notify (start_Lsp_Az); }  
  }  
  
  void Lsp_Az() {  
    while (true) {  
      wait(start_Lsp_Az);  
      initial_position = 1;  
      notify(start_Get_Lsp_pol);  
      for (i=5;i>0;i--) f1[i]=L_add(f1[i],f1[i-1]);  
      wait(start_Lsp_Az);  
      initial_position = 0;  
      for (i=5;i>0;i--) f2[i]=L_sub(f2[i],f2[i-1]);  
      . a is computed from f1 and f2  
    }  
  }  
}
```

```
Az_Lsp = mealyU(vf1, vf2, g, fi_p, fa, ω0)  
Az_Lsp(f1,f2) = <<initial_position><a>>  
if (statei=ω0) then  
  initial_positioni=fi_p(state)=1  
  //six 'f1' data are taken but no 'f2'  
  π(vf1, f1) = <f1i>  
  vf1(i) = 6  
  π(vf2, f2) = <f2i>  
  vf2(i) = 0  
  
  statei+1=ω1  
  
  //no 'a' data is generated  
  π(va, a) = <ai>  
  va(i) = 0  
else  
  initial_positioni=fi_p(state)=0  
  //six 'f2' data are taken but no 'f1' although 'f1 is used  
  π(vf1, f1) = <f1i>  
  vf1(i) = 0  
  π(vf2, f2) = <f2i>  
  vf2(i) = 6  
  
  statei+1=ω0  
  
  ai = fa(f1i,f2i)  
  //eleven 'a' data are generated  
  π(va, a) = <ai>  
  va(i) = 11
```

Formal Framework: Simple Example

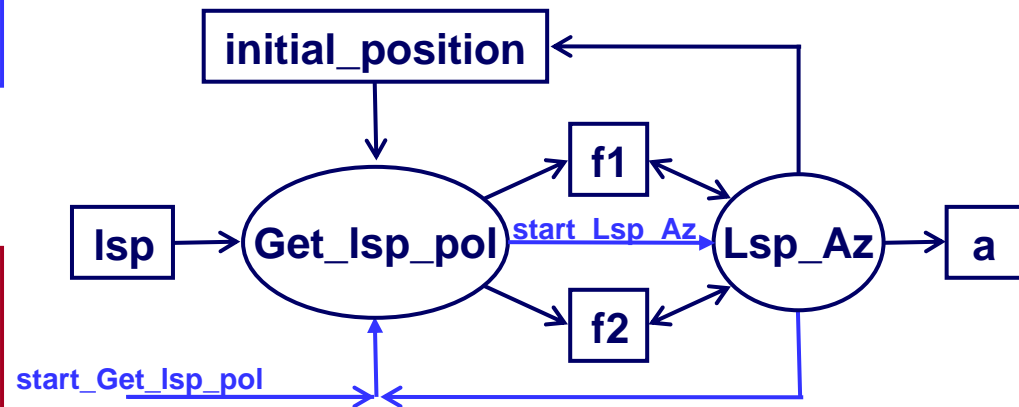


CSV1. Every data token written by the producer process is read by the consumer process.

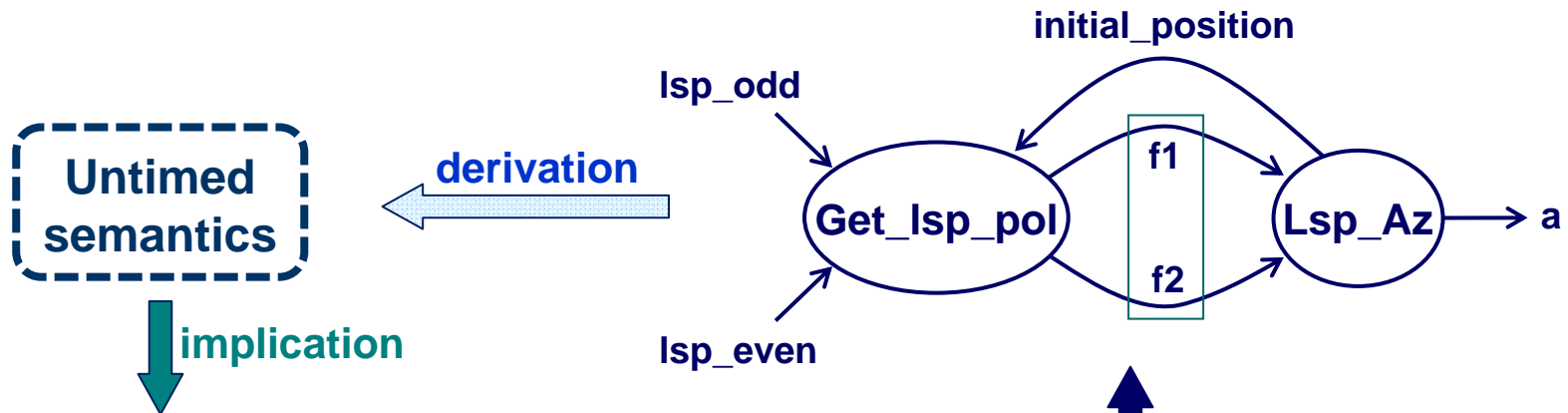
CSV2. Every data token written by the producer process is read only once by the consumer process.

design property

-- psl property CSV1_2_initial_position is always (initial_position.write_CALL() -> next(initial_position.read_CALL()) before initial_position.write_CALL());
-- psl assert CSV1_2_initial_position

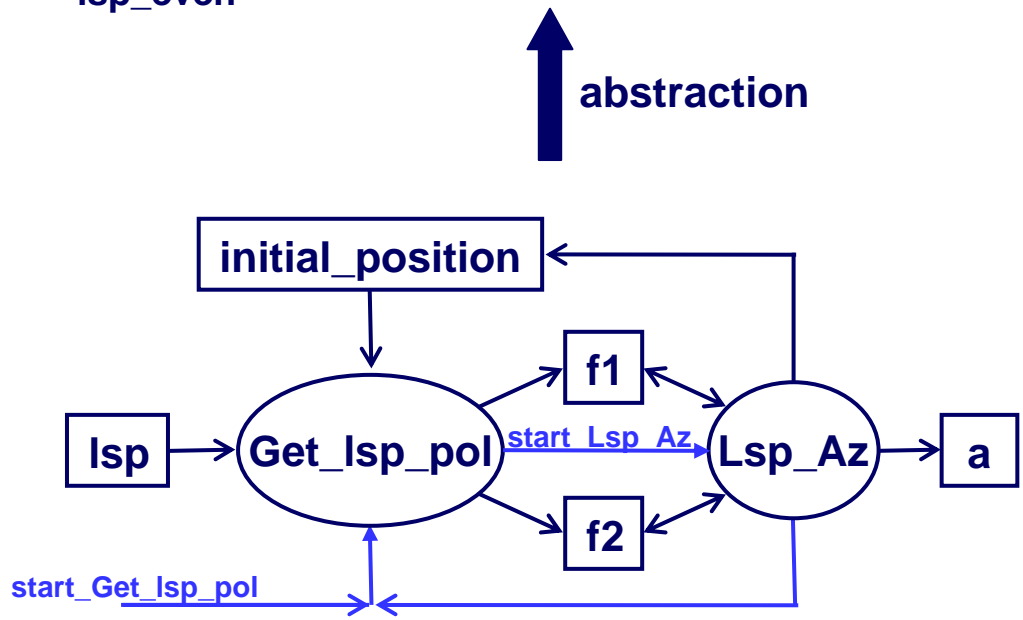


Formal Framework: Simple Example



implication

CSV3. If a consumer uses a shared variable as local memory, no new data can be written by the producer until the last access as local memory by the consumer, that is, during the local memory lifetime of the shared variable.



Application to High-Level Synthesis

- Synthesis results (after Gaut)

Strategy	Get_lsp_pol	Az_Lsp
Min. Area	1,740	810
Min. Latency	960	370

- Verification results
 - System verification testbench

Design	1	2	3	4
CSV1_2_initial_position	True	True	True	True
CSV1_2_f1	True	True	False	False
CSV1_2_f2	True	True	True	True
CSV3_f1	True	True	False	False
CSV3_f2	True	True	True	True
Functional correctness	OK	OK	Error	Error

Conclusions

- ForSyDe has been shown as a formal meta-model for SystemC
 - Untimed models
 - Specification semantics to be preserved
 - Application to high-level synthesis

Future Work

- Extended SystemC specification
 - More complex communication mechanisms
- Other applications
 - Architectural design
 - HW/SW mappings

Thanks and Questions

- Thank you for your attention

- Funding

