Motivation

The microprocessor will be the NAND gate of the integrated systems in 2010
- Alan Naumann, President and CEO, CoWare
- DATE’07
Motivation

- Simulation will remain a fundamental design tool
  - Functional validation
  - Performance estimation
  - Design-space exploration
  - Design verification
  - ...
Motivation

- Current ISS(+TLM) is too slow for
  - Functional verification
  - Performance estimation
  - Design-space exploration

- Only valid for final design verification
  - ISS+RTL(logic)
Motivation

- SW execution is only valid for
  - Initial functional validation
  - Temporal behavior missed
Contents

- SScope description
  - Goals
  - Features
  - Platform model
  - Power estimation
- Application example
- Conclusions
SScope: Goal

- HW/SW simulation platform for MpSoC with NoC
- Performance estimation
- Power estimation
- Fast
- As accurate as possible
SCope: Features

- SW source-code simulation
  - Two orders of magnitude faster than ISS
- Abstract RTOS model
- Abstraction of the microprocessor
- Timed simulation
  - Performance estimation
- Power consumption estimation
SCope: Features (cont.)

- HW TLM(RTL) models
- HW/SW communication
  - Interruptions
  - Drivers
- TLM2 Bus model
- DMA
- NoC Interface
SCope: Platform model

- Application Code
  - Task 1 ... Task n
- POSIX API
- Packages
- Drivers

- Memory
- Proc. 1
- Proc. 2
- Proc. n
- Bus 1
- Bus n
- Net Per.
- Application-specific HW
- Peripheral

SW

HW
SCope: RTOS modeling

SW Platform

- Applic. Code
  - T1
  - T2
  - Tn

- OS API (POSIX)
- Spec. I/O

- OS Core
- External Packs (TCP/IP)
- Drivers

- Low-level HAL

OS API

- Communication
- Synchronization
- Concurrency
- Memory management
- Scheduling

Low-level HAL

- Interruptions
- Module Loading
- File system
- BUS Access
- Devices
PERFidiX: HAL Modeling

- HW/SW communication
  - Drivers
    - Linux functions for drivers development
    - File system control and device management
  - Bus Access
    - Reading and writing
      - memory and peripherals
  - Interruptions
    - IRQ from HW platform
    - Interrupt managers and masks
PERFidiX: SW Packages

- POSIX-based RTOS allow inclusion of standard packages
  - Stack TCP/IP: lwIP
    - Reduced memory requirements
    - Several protocols implemented
      - IP, ICMP, UDP, TCP, DHCP, ARP, ...
    - Uses a Ethernet driver model
      - Connected using the network simulator
  - Work in progress
PERFidiX: Execution time and Energy estimation

Dynamic Time & Power Estimation

<table>
<thead>
<tr>
<th>Operation</th>
<th>Time</th>
<th>Total</th>
<th>Energy</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>a = b + d ;</td>
<td>2+7 us</td>
<td>9 us</td>
<td>2+5 uJ</td>
<td>7 uJ</td>
</tr>
<tr>
<td>c = a*b ;</td>
<td>2+68 us</td>
<td>79 us</td>
<td>2+40 uJ</td>
<td>49 uJ</td>
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<tr>
<td>d = a;</td>
<td>2 us</td>
<td>81 us</td>
<td>2 uJ</td>
<td>51 uJ</td>
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<tr>
<td>if ( c &lt; 0 )</td>
<td>20+18 us</td>
<td>119 us</td>
<td>20+10 uJ</td>
<td>81 uJ</td>
</tr>
<tr>
<td>a = c + 1 ;</td>
<td>2+7 us</td>
<td>128 us</td>
<td>2 + 5 uJ</td>
<td>88 uJ</td>
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<tr>
<td>Total seg.</td>
<td>128 us</td>
<td></td>
<td></td>
<td>687 mW</td>
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OPERATOR

<table>
<thead>
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<tbody>
<tr>
<td>=</td>
<td>2 us</td>
<td>2 uJ</td>
</tr>
<tr>
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<td>7 us</td>
<td>5 uJ</td>
</tr>
<tr>
<td>*</td>
<td>68 us</td>
<td>40 uJ</td>
</tr>
<tr>
<td>&lt;</td>
<td>20 us</td>
<td>20 uJ</td>
</tr>
<tr>
<td>IF</td>
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</table>
PERFidiX: Power estimation

- Standard RISC processors exhibit stable power consumption per instruction
- Dynamic simulation allows estimating energy consumption
  - number of assembler instructions executed
  - energy cost per instruction
- Power estimation
  - energy/execution times
- Adaptive dynamic voltage-frequency scaling
SCope: BUS modeling

- Data Transfers
  - payload (faster than word by word)
- Interruptions
- TLM2
- Models
  - Several masters
  - Several slaves
  - Bus chaining
  - Stop / Abort
SCope: Generic peripheral interface

- Bus protocol management
  - Implements transport & send interrupt
  - Manages Stop and Abort operations
  - Waits corresponding time
    - bandwidth and delay
- Integrated using inheritance
  - Allows modifying protocol management in a specific peripheral
  - Protocol functionality integrated in the peripheral
  - Declare bus ports automatically (SC_EXPORT)
SCope: Specific Peripheral models

- Network Interface
  - Connects the bus and the NoC model
  - Acts as slave
  - Informs the processor through interrupts

- DMA
  - Master / Slave
  - Moves payloads between other peripherals

- Memory
  - Allows modeling bus loads of data transfers
    - processor-memory and DMA-memory
SCope: Network Modeling

- Network on Chip simulator: Sicosys
  - University of Cantabria (UC-ATC)
  - Based on models of the NoC components
  - Several NoC configurations
- Integrated as a SystemC Thread
- Computes when packages are in the NoC
  - Otherwise Stopped
Example: Vocoder GSM

- Two nodes connected through a NoC

Node 1:
- Coder
- Proc.
- Memory
- BUS
- I/O
- NoC IF.

Node 2:
- Decoder
- Proc.
- Memory
- BUS
- NoC IF.
- I/O

NoC
Example: Platform model
Example: Performance Analysis

- SW execution times
  - Thread statistics
  - Power consumption

- Bus statistics
  - Contentions
  - Conflicts

- Network
  - Delays
  - Latencies
Example: Performance Analysis
Conclusions

- **SystemC**
  - powerful framework for complex SoC with NoC modeling

- **SCope**
  - Multiprocessing SW simulation
  - SW power consumption
  - Platform modeling
    - Bus, DMA, AS-HW, Memory, NoC IF, ...
  - NoC simulation
  - Sicosis