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SW simulation and Performance Analysis

In Multi-Processing Embedded Systems

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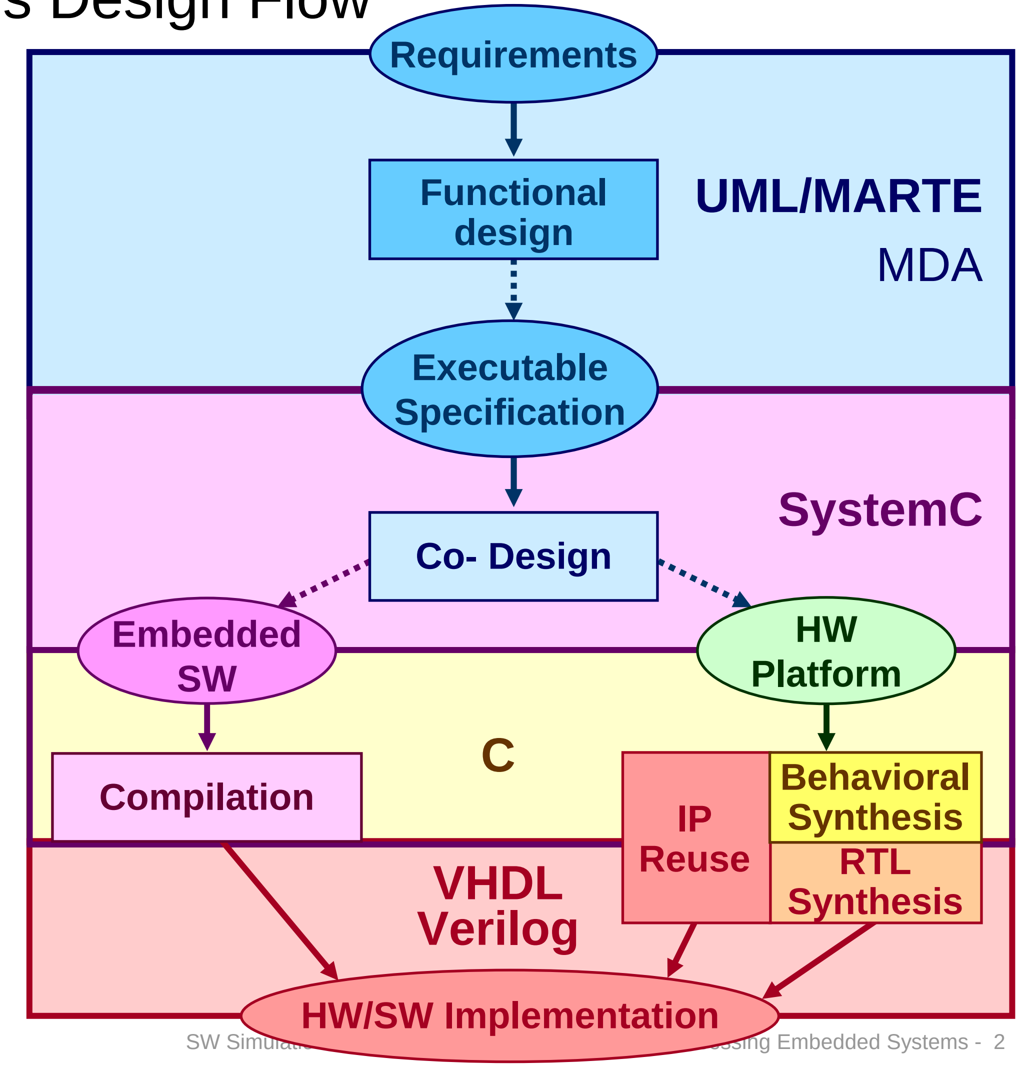
Advanced Research & Technology for EMbedded Intelligence and Systems

Context

- HW/SW Embedded Systems Design Flow
  - HW/SW Simulation
  - Performance Analysis
  - Design Verification
    - At the different abstraction levels



Requirements

Functional design

UML/MARTE

MDA

Executable Specification

SystemC

Co- Design

Embedded SW

HW Platform

C

Compilation

IP Reuse

Behavioral Synthesis

RTL Synthesis

VHDL Verilog

HW/SW Implementation

Agenda

- Motivation: Why SW simulation
- Technologies: How SW simulation
- SCoPE: SW simulation for DSE
  - SW performance analysis
  - Improvements for Scalopes
- Conclusions

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Motivation

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Motivation

- The MPSoC
  - Multi-processing platform
    - ASIC
    - FPGA
    - Commercial multi-processing platform
  - SW-centric design methodology
    - Most of the functionality implemented as Embedded SW
    - With ‘some’ application-specific HW

Motivation

- Software Reliability

WASHINGTON (COMPUTERWORLD) - Software bugs are costing the U.S. economy an estimated $59.5 billion each year, with more than half of the cost borne by end users and the remainder by developers and vendors, according to a new federal study.

Improvements in testing could reduce this cost by about a third, or $22.5 billion, but it won't eliminate all software errors, the study said. Of the total $59.5 billion cost, users incurred 64% of the cost and developers 36%.

In Embedded SW both Functionality and Performance are relevant

- http://www.cse.lehigh.edu/~gtan/bug/softwarebug.html
- http://www.sereferences.com/software-failure-list.php
- http://www5.in.tum.de/~huckle/bugse.html ...

Motivation

- Embedded SW simulation
  - As an integral part of the MPSoC simulation
  - Essential for MPSoC verification
    - At any abstraction level
  - Essential for DSE
    - During architectural design
  - Essential for performance analysis
    - At any abstraction level

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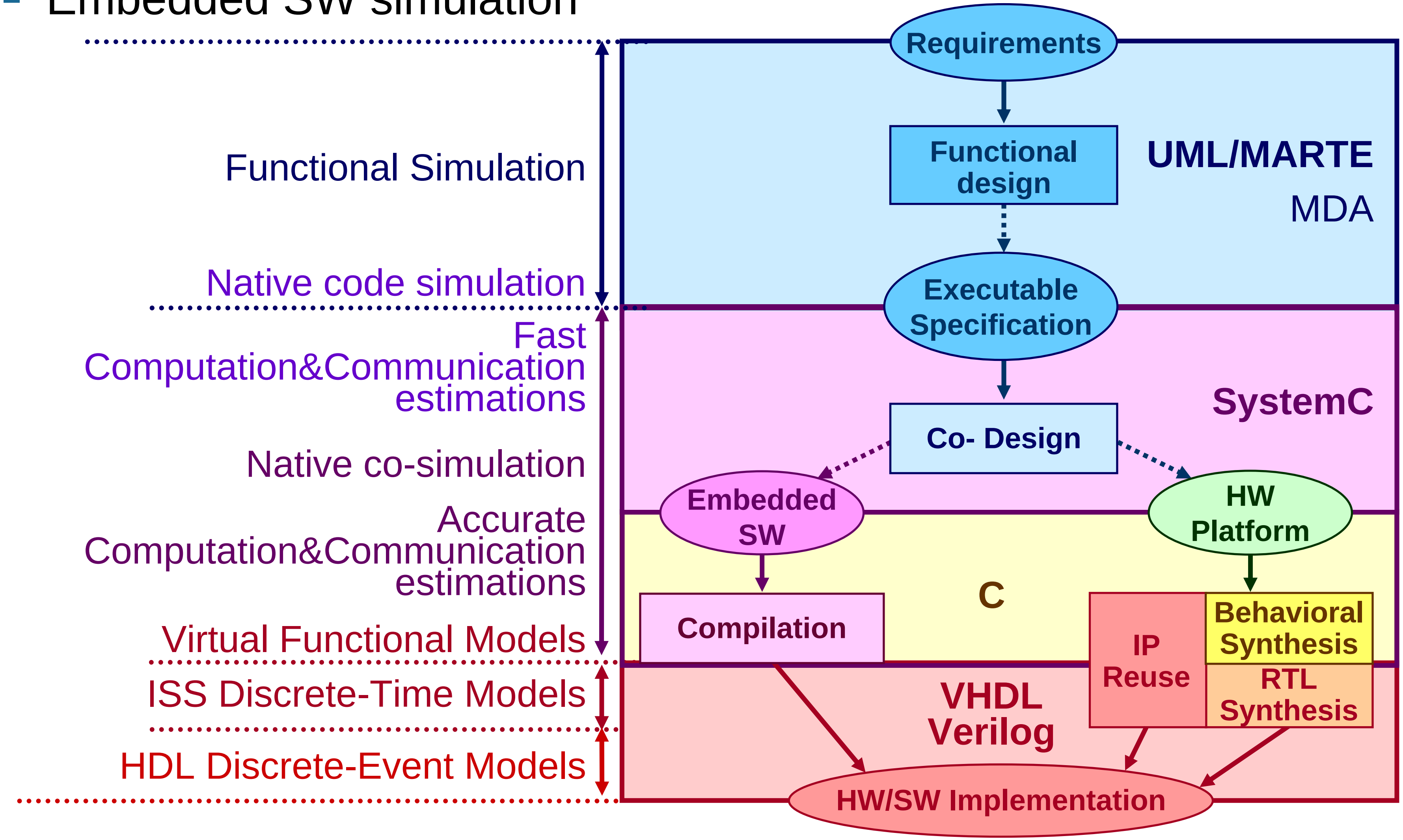
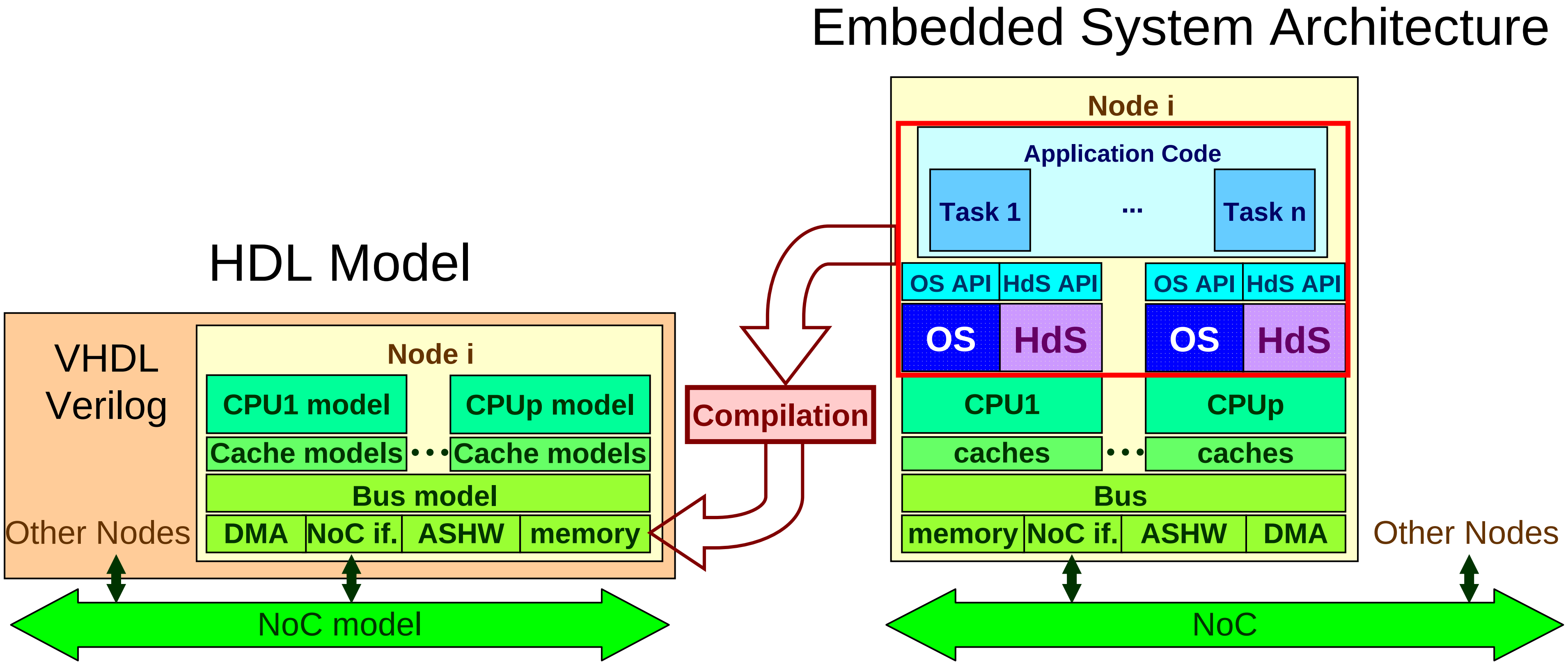
Embedded SW simulation technologies

- Embedded SW simulation



Embedded SW simulation technologies

- HDL simulation

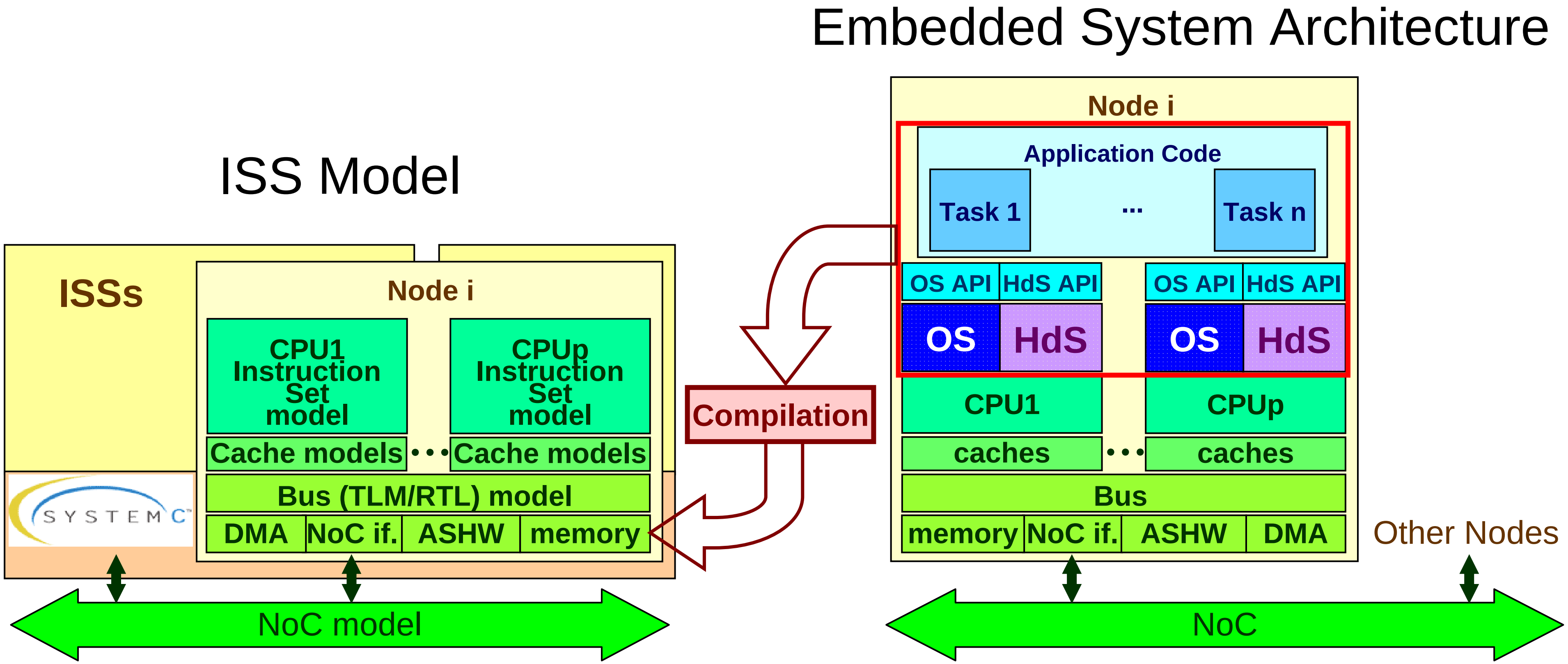


Embedded SW simulation technologies

- HDL simulation
  - Very detailed model
    - High modeling cost
    - Late design steps
  - Highest accuracy
    - Discrete delays
  - Highest simulation times

Embedded SW simulation technologies

- ISS simulation

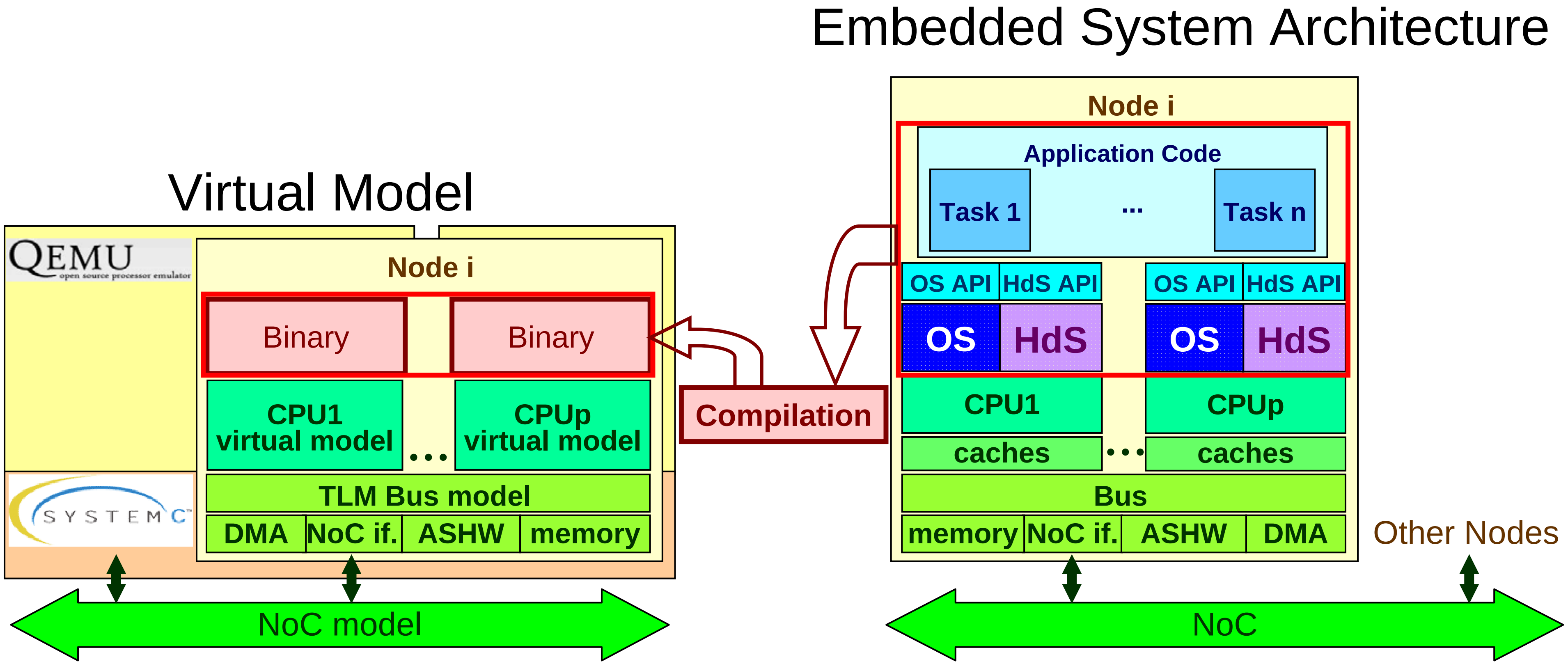


Embedded SW simulation technologies

- ISS simulation
  - Detailed model
    - High modeling cost
    - Late design steps
  - Cycle accuracy
  - High simulation times

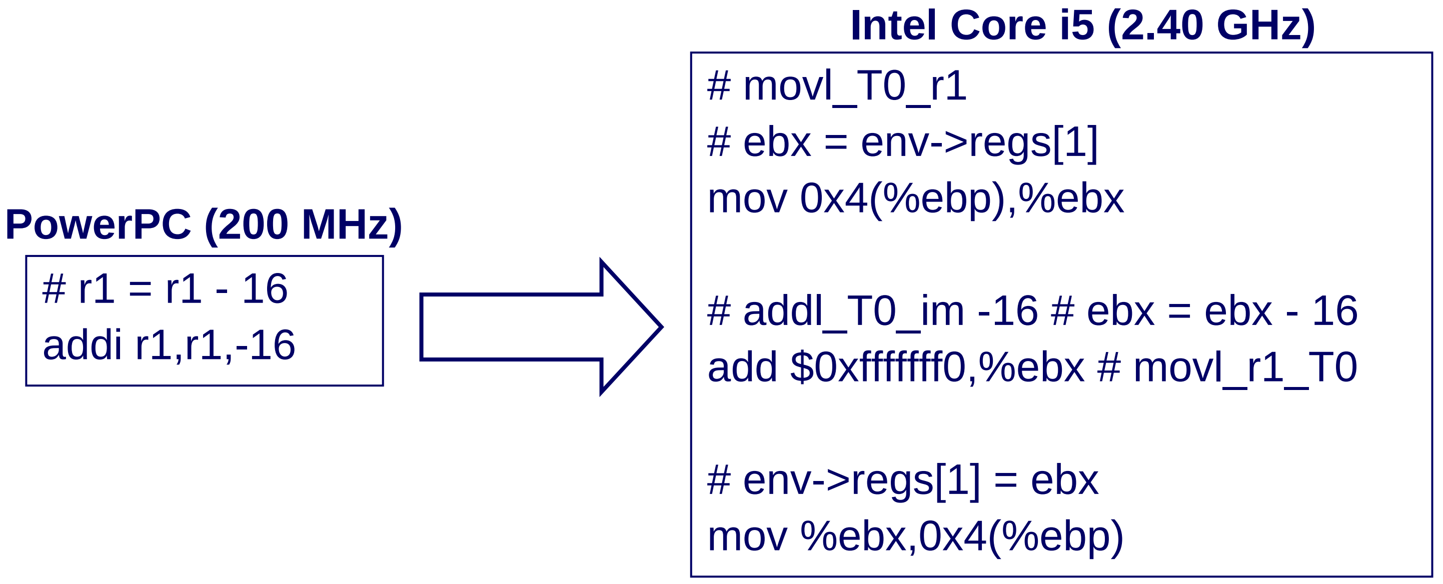
Embedded SW simulation technologies

- Virtualization



Embedded SW simulation technologies

- Virtualization (QEMU)
  - Detailed model
    - High modeling cost
    - Late design steps
  - High simulation times
    - Faster than ISS



PowerPC (200 MHz)

```
# r1 = r1 - 16
addi r1,r1,-16
```

Intel Core i5 (2.40 GHz)

```
# movl_T0_r1
# ebx = env->regs[1]
mov 0x4(%ebp),%ebx

# addl_T0_im -16 # ebx = ebx - 16
add $0xfffffff0,%ebx # movl_r1_T0

# env->regs[1] = ebx
mov %ebx,0x4(%ebp)
```

Embedded SW simulation technologies

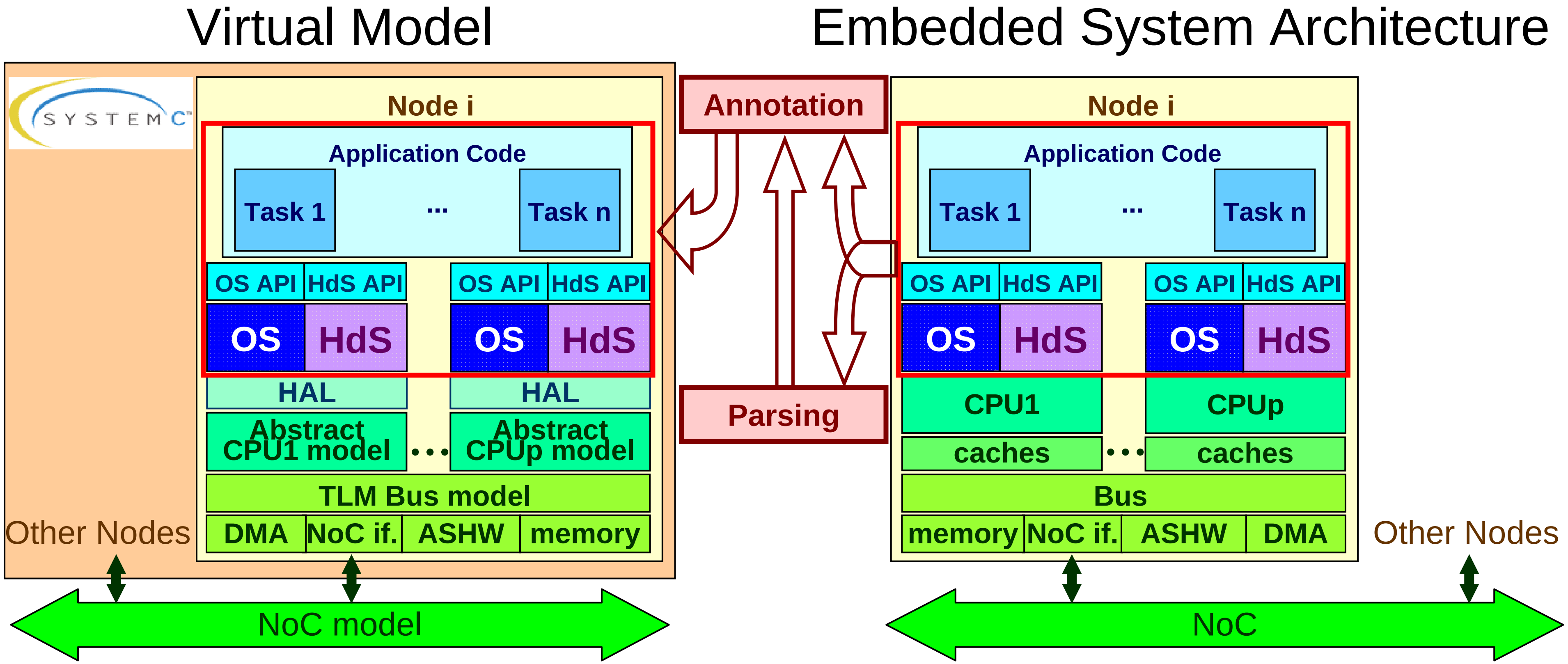
- Virtualization (QEMU)
  - ➢ Functional emulation
  - ➢ Rough timed simulation
    - i.e. 1 cycle per instruction
  - ➢ Large effort needed for more accurate modeling
    - Execution times
    - Power consumption
    - Caches
    - …
  - ➢ Requires a specific Virtual Model for each processor

Embedded SW simulation technologies

- Native simulation
  - Embedded code directly executed by the host
  - Good accuracy by back-annotation
  - Fast execution time

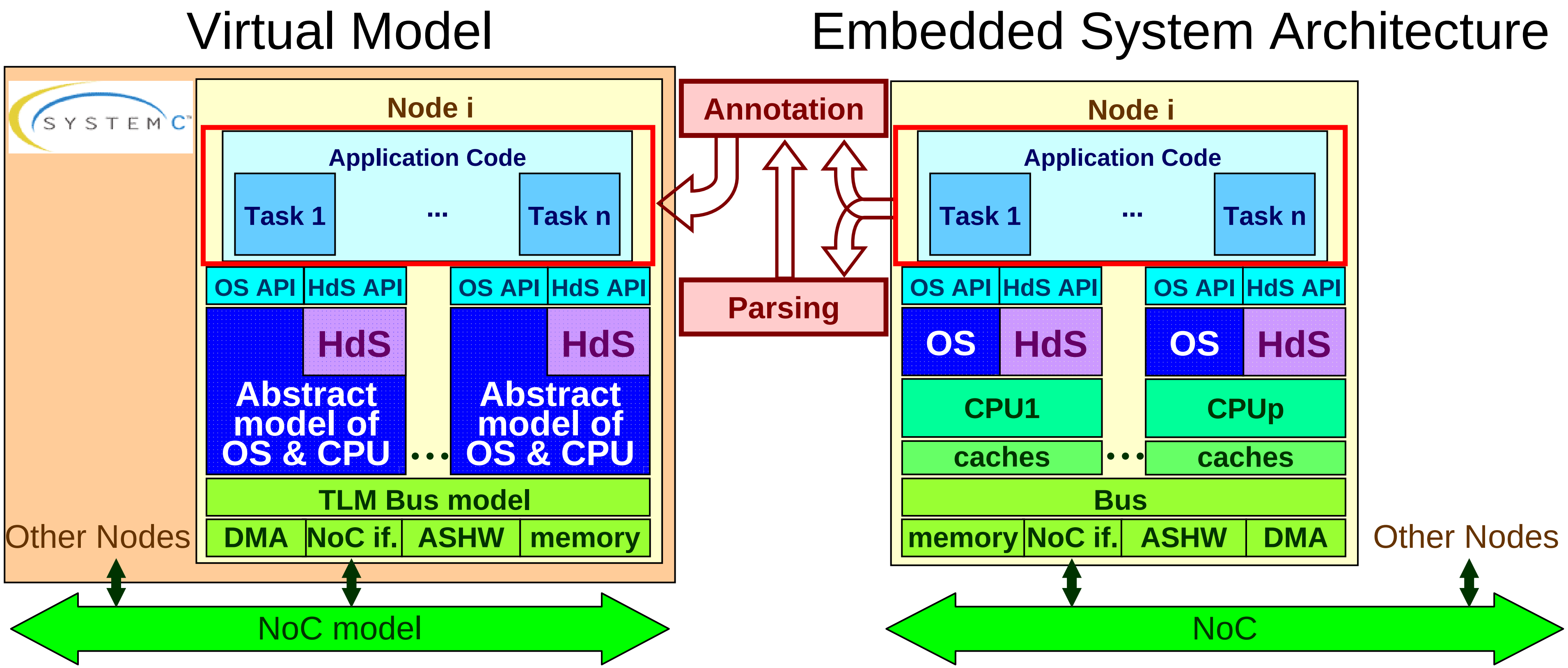
Embedded SW simulation technologies

- Native simulation based on HAL API



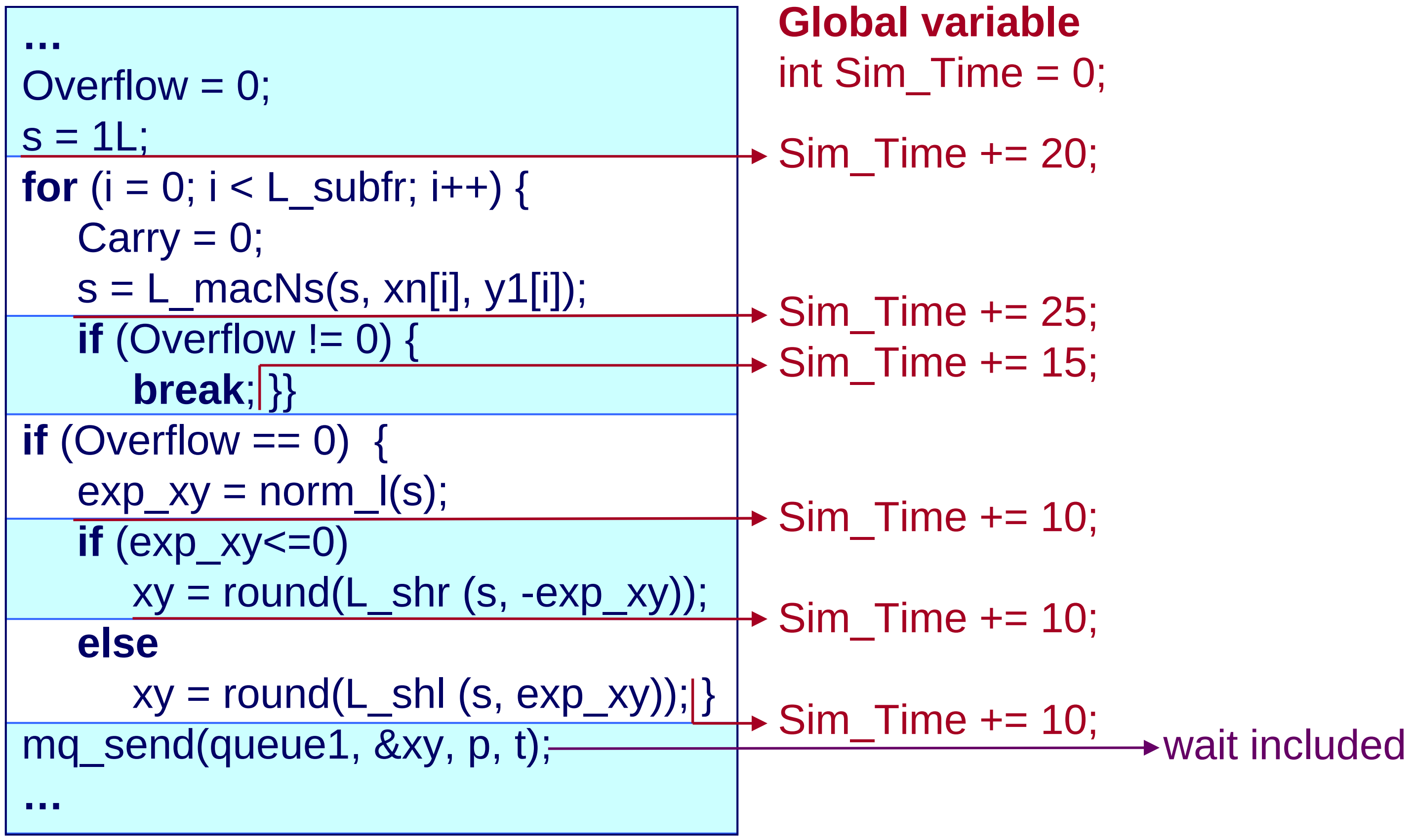
Embedded SW simulation technologies

- Native simulation based on OS API



Embedded SW simulation technologies

- Code annotation in native simulation



```
…
Overflow = 0;
s = 1L;
for (i = 0; i < L_subfr; i++) {
    Carry = 0;
    s = L_macNs(s, xn[i], y1[i]);
    if (Overflow != 0) {
        break;}}
if (Overflow == 0)  {
    exp_xy = norm_l(s);
    if (exp_xy<=0)
        xy = round(L_shr (s, -exp_xy));
    else
        xy = round(L_shl (s, exp_xy));}
mq_send(queue1, &xy, p, t);
…
```

Global variable

int Sim_Time = 0;

Sim_Time += 20;

Sim_Time += 25;

Sim_Time += 15;

Sim_Time += 10;

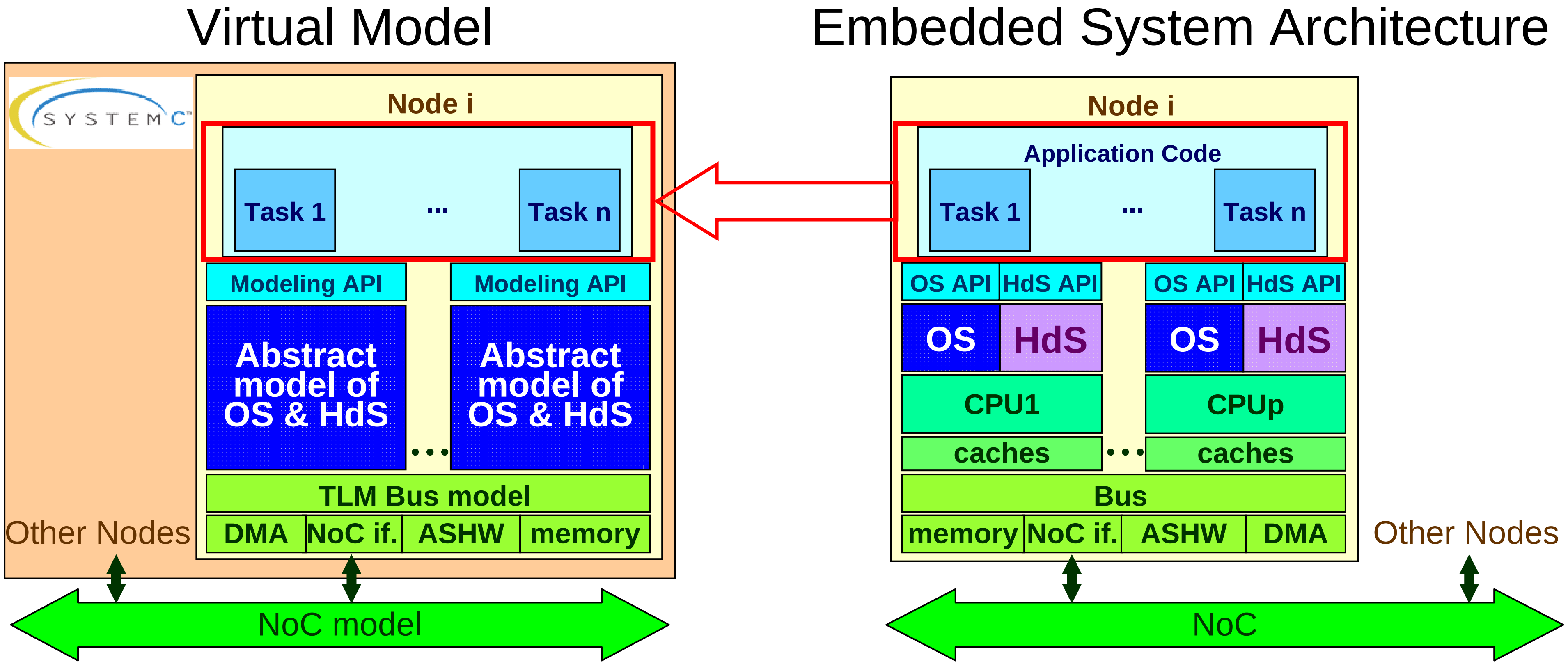
Sim_Time += 10;

Sim_Time += 10;

wait included

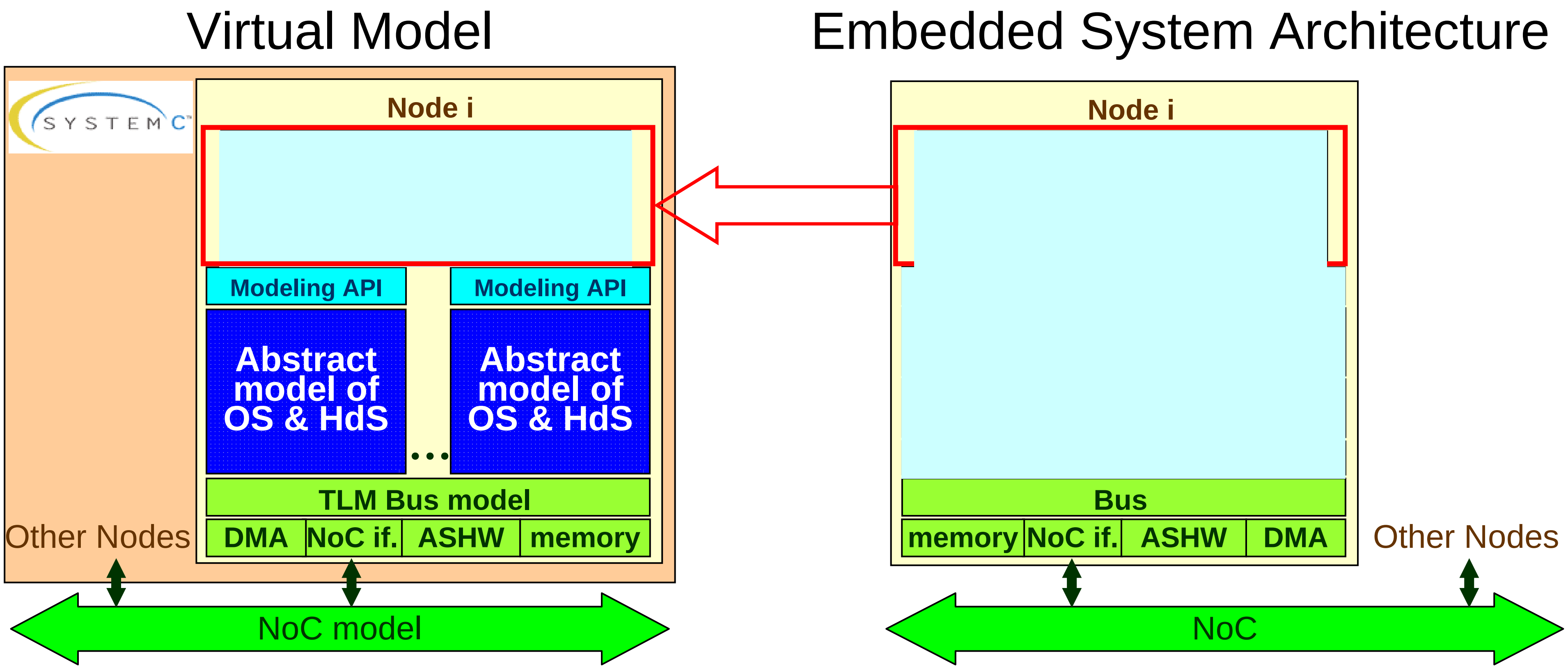
Embedded SW simulation technologies

- Functional simulation based on code



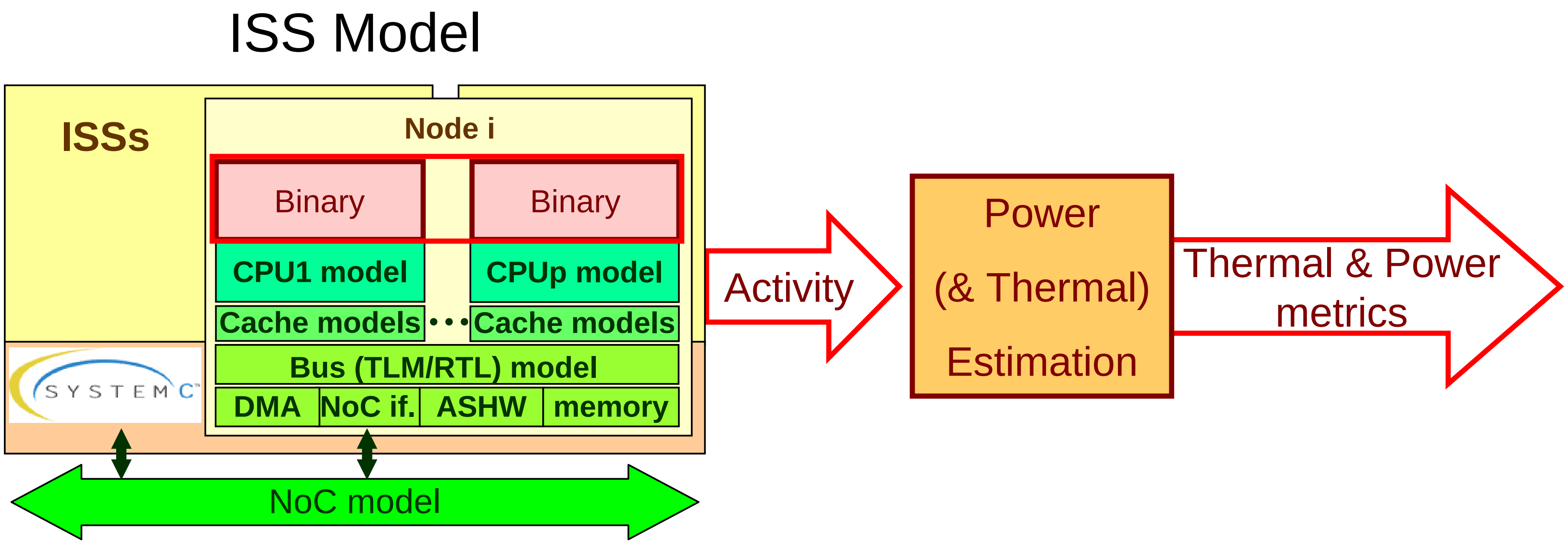
Embedded SW simulation technologies

- Functional simulation based on abstract tasks



Embedded SW simulation technologies

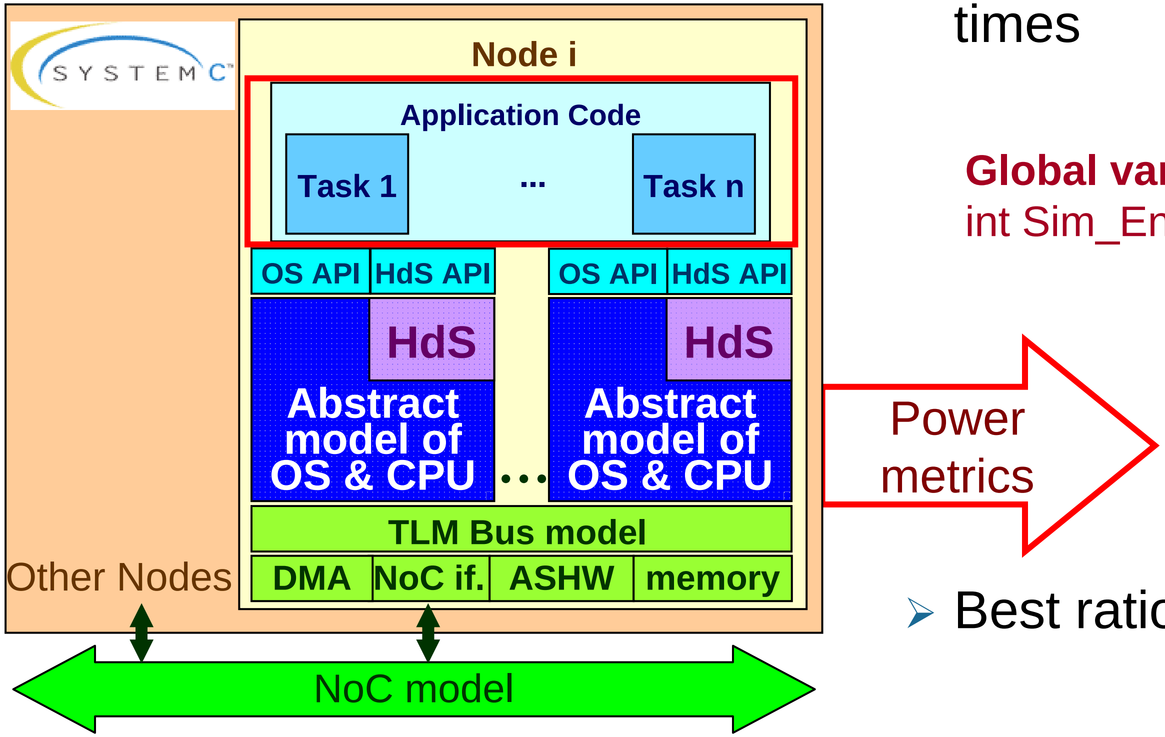
- Power estimation based on traces
  - Accurate but slow



Embedded SW simulation technologies

- Power estimation based on back-annotation

Virtual Model



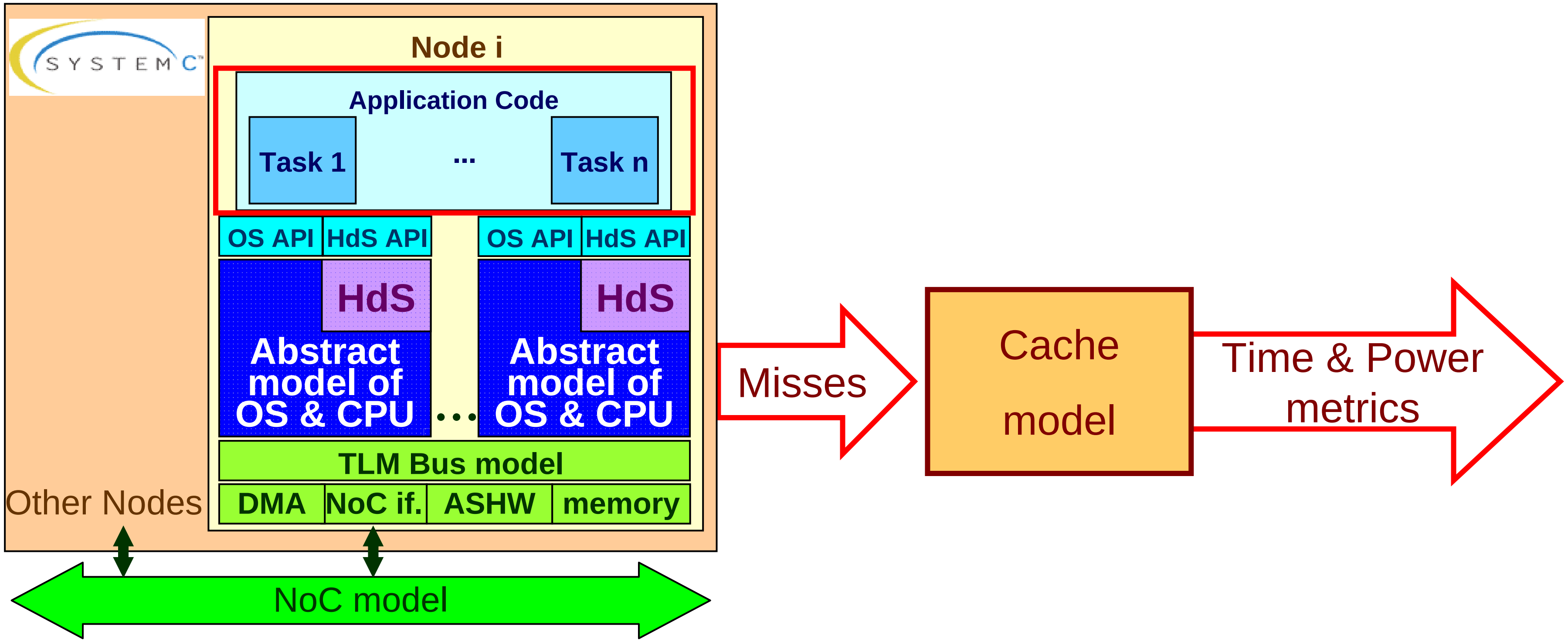
- Same technology as with execution times

Global variable
int Sim_Energy = 0;

- Best ratio accuracy/speed

Embedded SW simulation technologies

- Cache modeling



Embedded SW simulation technologies

- Performance/Error comparison

Technology		Time Estimation	Time & Power Estimation
Functional	Performance	5,000	N.A.
	Error	N.A.	N.A.
Native	Performance	1,000	500
	Error	1.3	1.4
Virtualization	Performance	200	T.B.M.
	Error	1.5	T.B.M.
ISS (cycle-accurate)	Performance	10	1
	Error	1.1 (DT)	1.1
HDL	Performance	1	0.1
	Error	1 (DE)	1

- Rough approximate figures

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SCoPE: SW Performance Modeling

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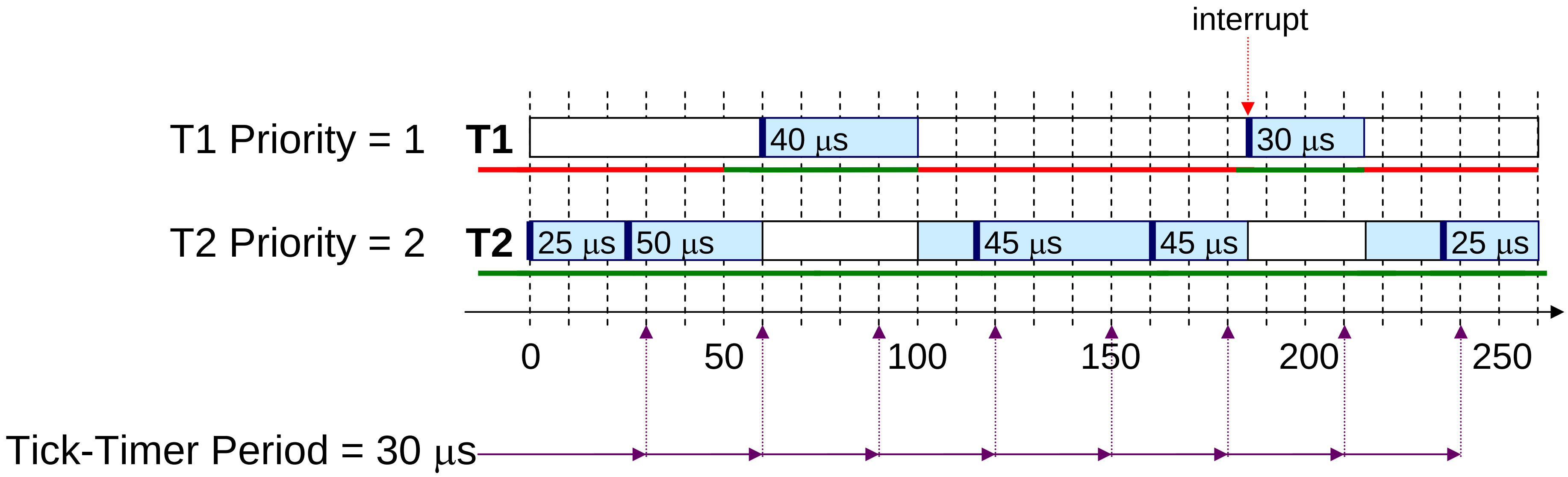
SCoPE: SW Performance Estimation

- Key features
  - Abstract OS modeling
  - Instruction cache modeling

- Novel features
  - Physical memory accesses
  - Separate memory spaces
  - Design-space exploration

SCoPE: SW Performance Estimation

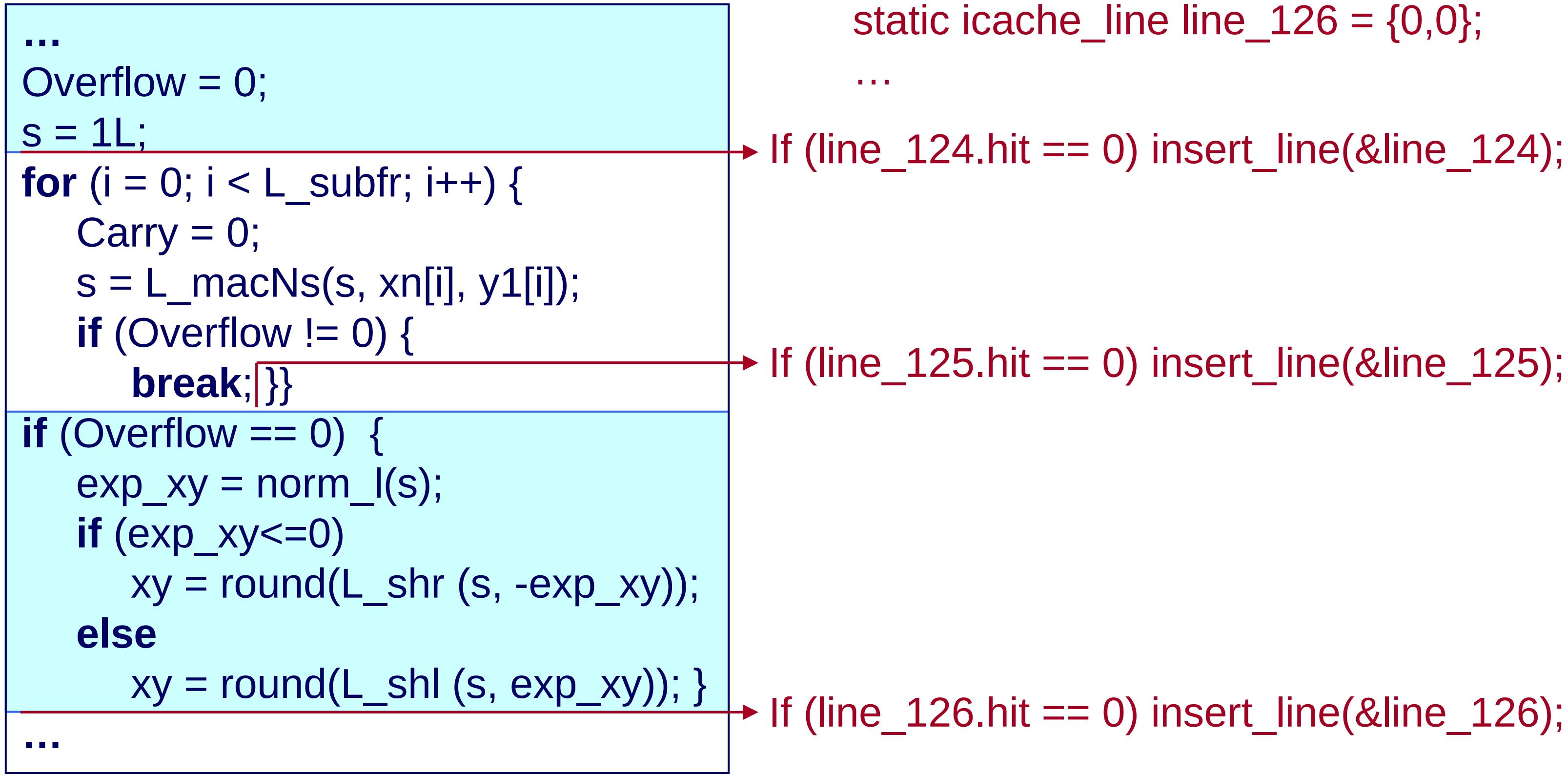
- Abstract OS modeling
  - POSIX threads modeled as SC_THREADs
  - Scheduler model
  - Time modeling
  - RTOS services (POSIX & μCOS APIs)



SCoPE: SW Performance Modeling

- Instruction cache modeling
  - Similar to time modeling

```
struct icache_line {  char num_set; char hit; }
…
static icache_line line_124 = {0,0};
static icache_line line_125 = {0,0};
static icache_line line_126 = {0,0};
…
```



```
…
Overflow = 0;
s = 1L;
for (i = 0; i < L_subfr; i++) {
    Carry = 0;
    s = L_macNs(s, xn[i], y1[i]);
    if (Overflow != 0) {
        break; }}
if (Overflow == 0)  {
    exp_xy = norm_l(s);
    if (exp_xy<=0)
        xy = round(L_shr (s, -exp_xy));
    else
        xy = round(L_shl (s, exp_xy)); }
…
```

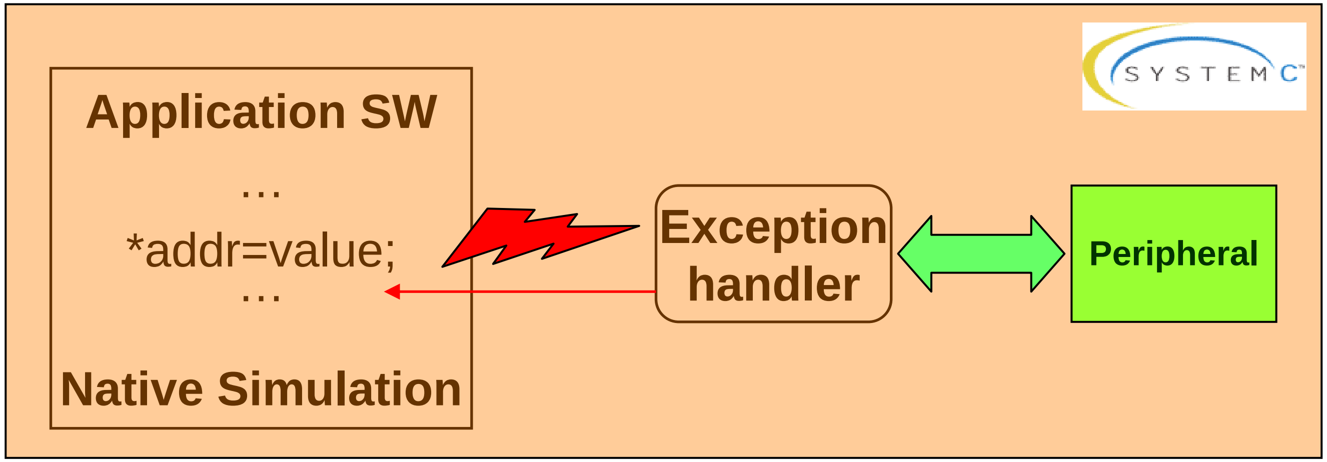
```
If (line_124.hit == 0) insert_line(&line_124);
If (line_125.hit == 0) insert_line(&line_125);
If (line_126.hit == 0) insert_line(&line_126);
```

SCoPE: SW Performance Modeling

- Physical memory accesses
  - Memory (re)map for passive accesses

```
pa=mmap(addr, len, prot, flags, fildes, off);
```

  - Access to peripherals



SCoPE: SW Performance Modeling

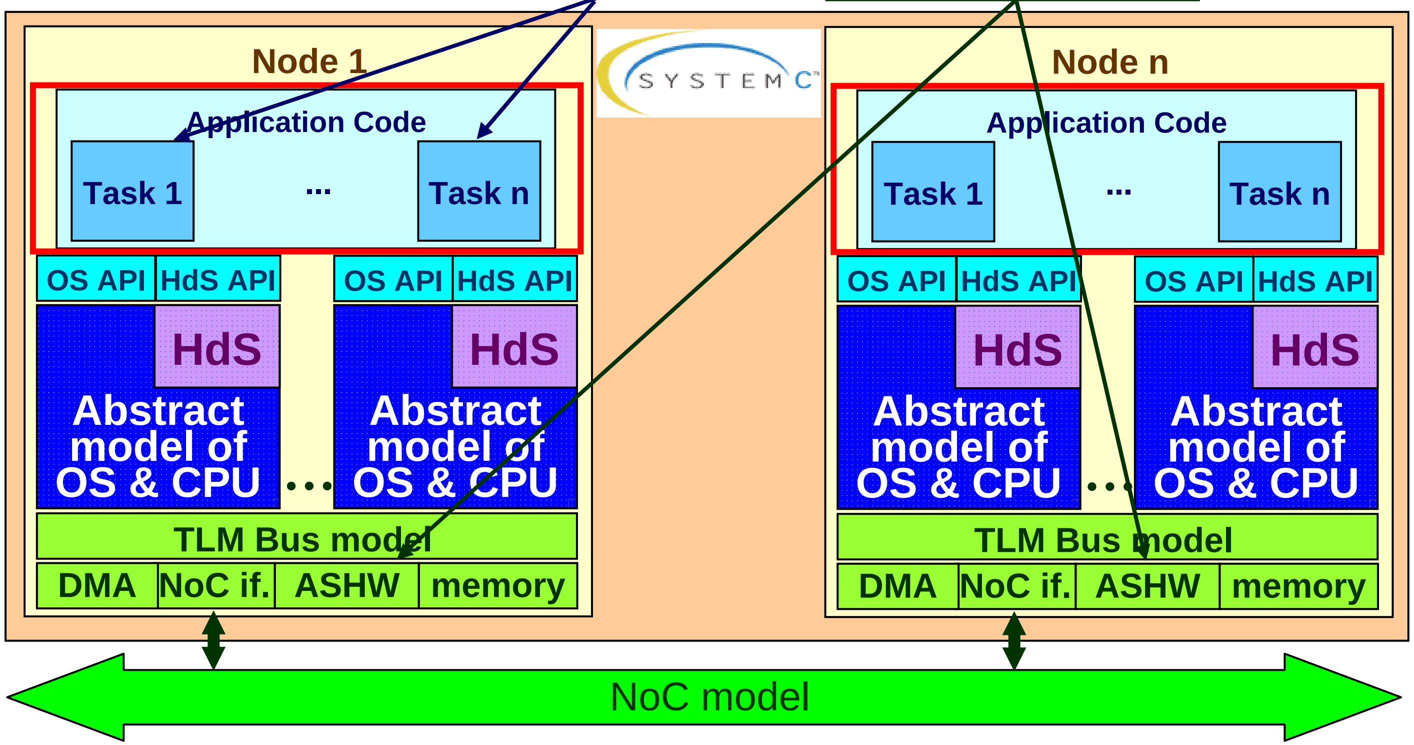
- Separate memory spaces
  - Use of dynamic libraries

Task T

```
int global = 0;
void func() {
…
{
int main() {
…
}
```

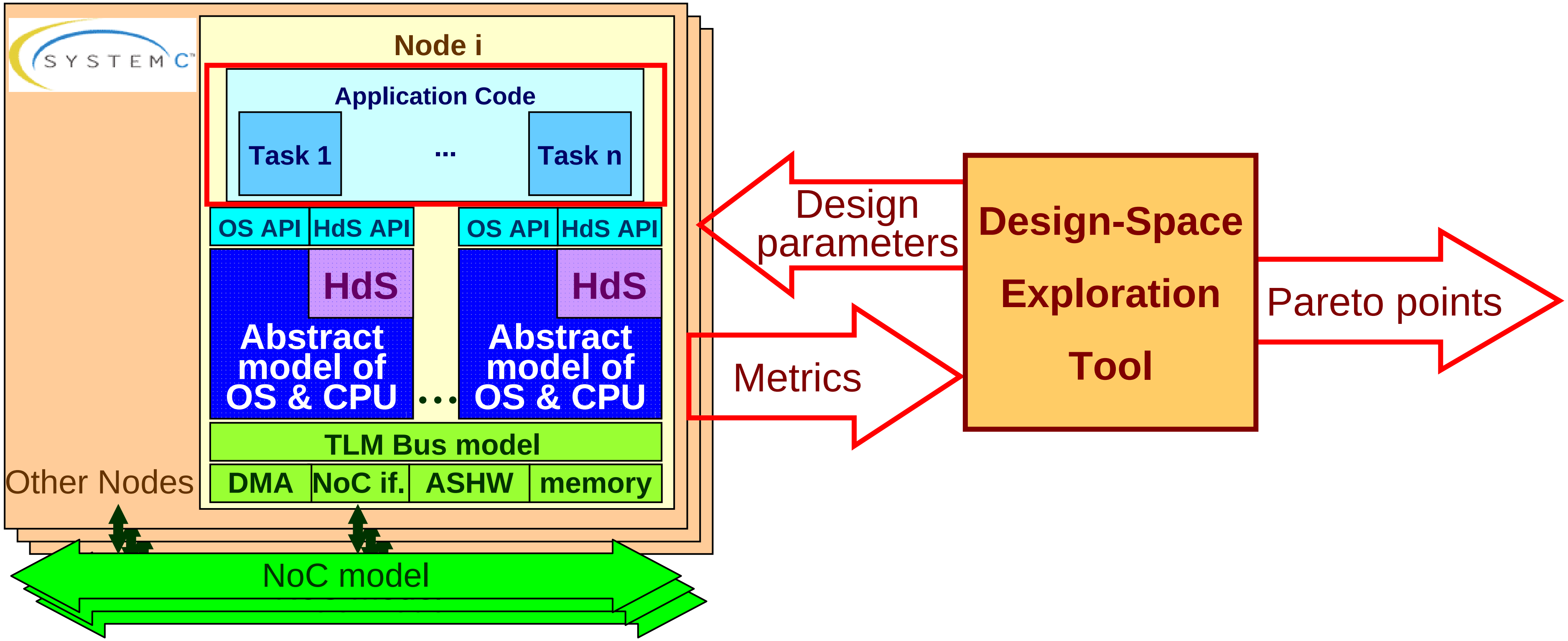
Peripheral P

```
int regs[4];
void read_reg() {
…
{
int write_reg() {
…
}
```



SCoPE: SW Performance Modeling

- Design-Space Exploration
  - Configurable model



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SCoPE: Improvements for Scalopes

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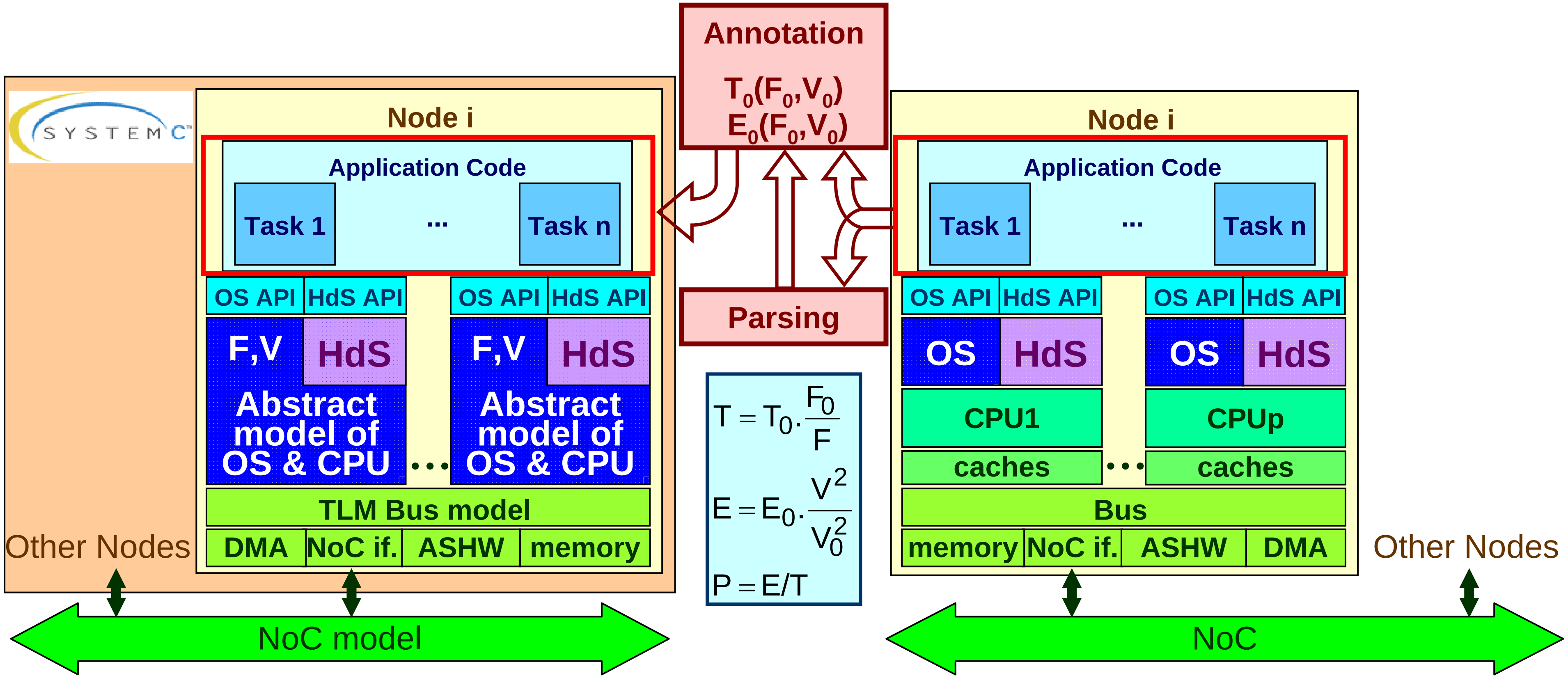
SCoPE: Improvements for Scalopes

- Dynamic Voltage-Frequency Scaling



Annotation

$T_0(F_0,V_0)$
$E_0(F_0,V_0)$

Parsing

$$T = T_0 \cdot \frac{F_0}{F}$$

$$E = E_0 \cdot \frac{V^2}{V_0^2}$$

$$P = E/T$$

SYSTEMC

Node i

Application Code

Task 1 ... Task n

OS API | HdS API | OS API | HdS API

F,V | HdS | F,V | HdS

Abstract model of OS & CPU ... Abstract model of OS & CPU

TLM Bus model

DMA | NoC if. | ASHW | memory

Other Nodes

NoC model

Node i

Application Code

Task 1 ... Task n

OS API | HdS API | OS API | HdS API

OS | HdS | OS | HdS

CPU1 ... CPUp

caches ... caches

Bus

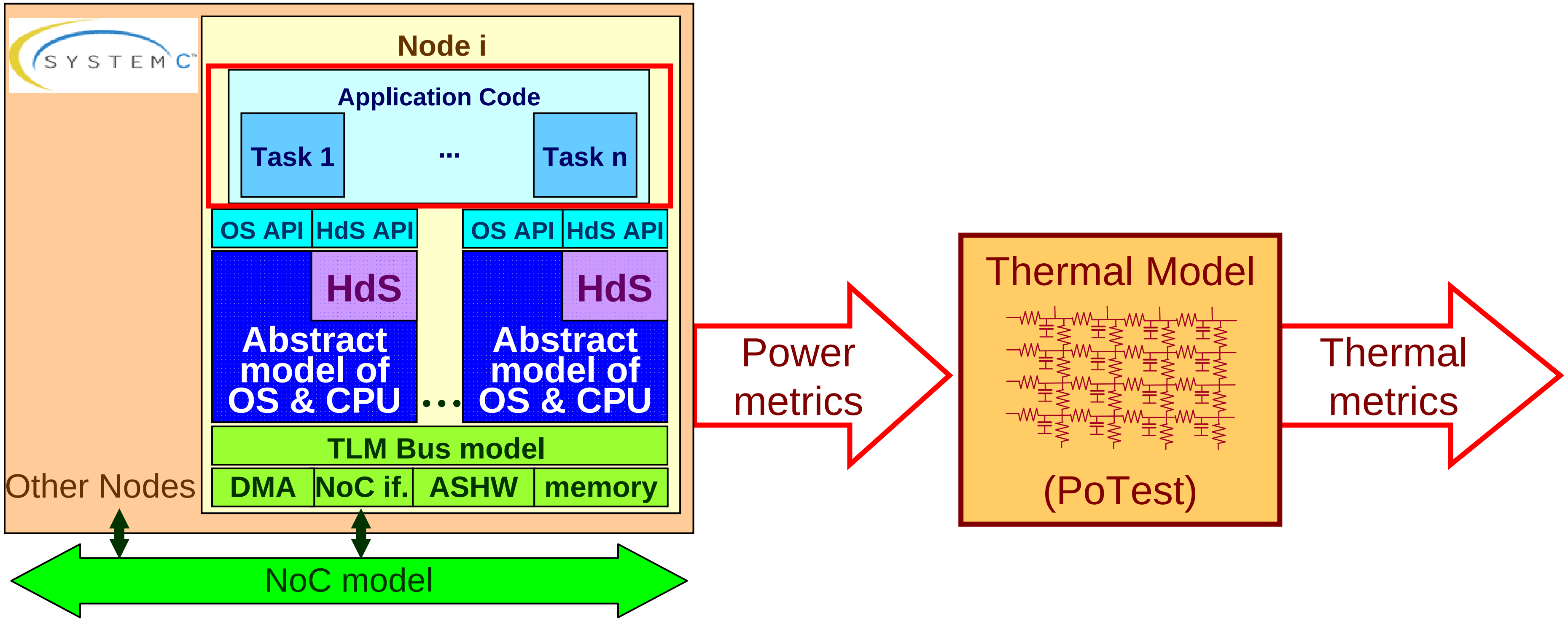
memory | NoC if. | ASHW | DMA

Other Nodes

NoC

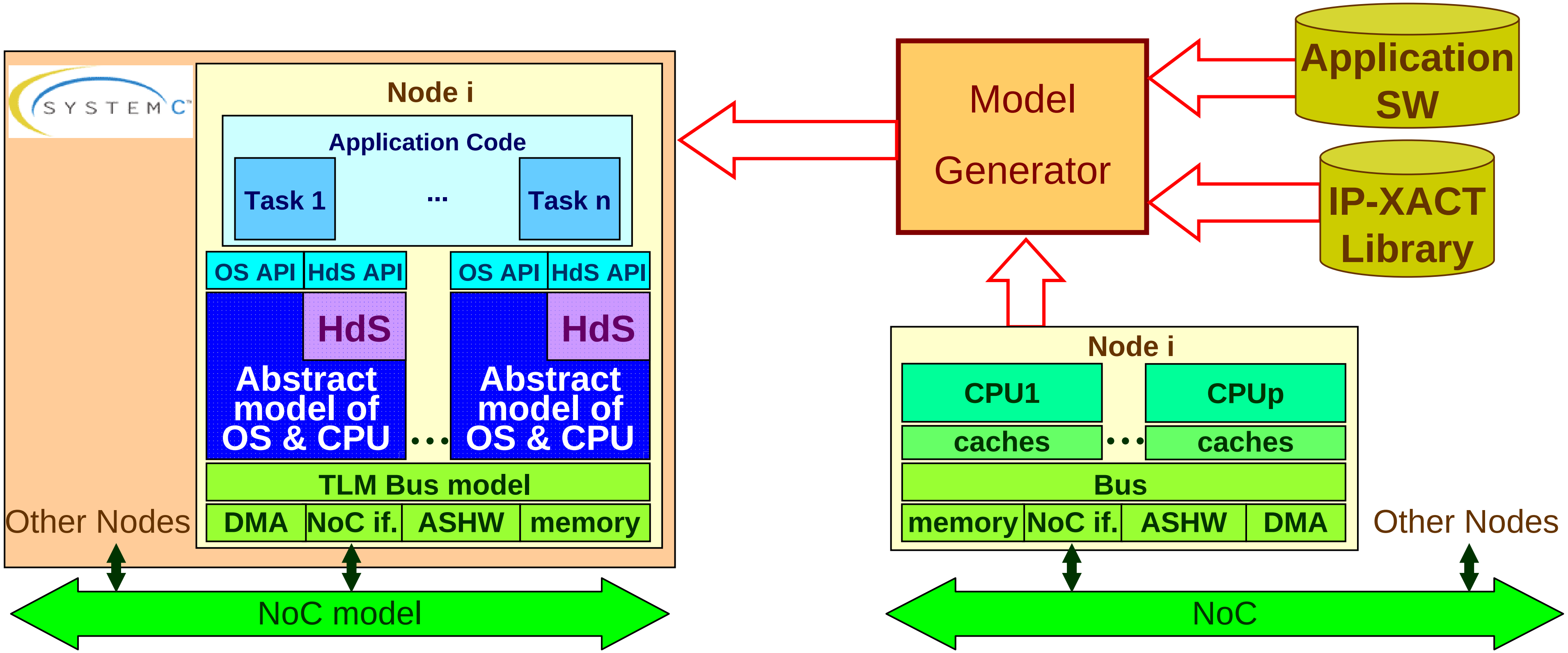
SCoPE: Improvements for Scalopes

- Thermal modeling



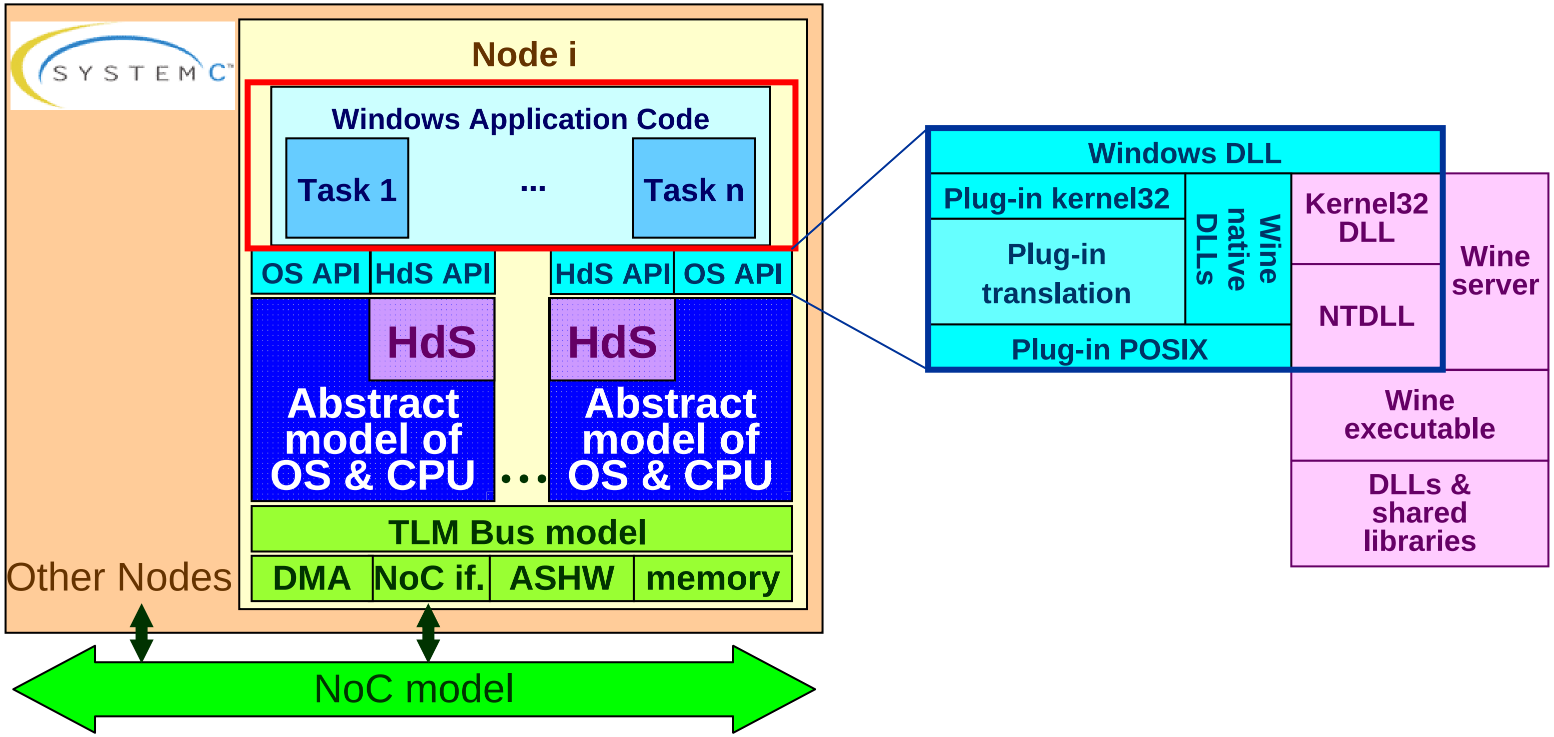
SCoPE: Improvements for Scalopes

- System composition from IP-XACT components



SCoPE: Improvements for Scalopes

- WIN32 API

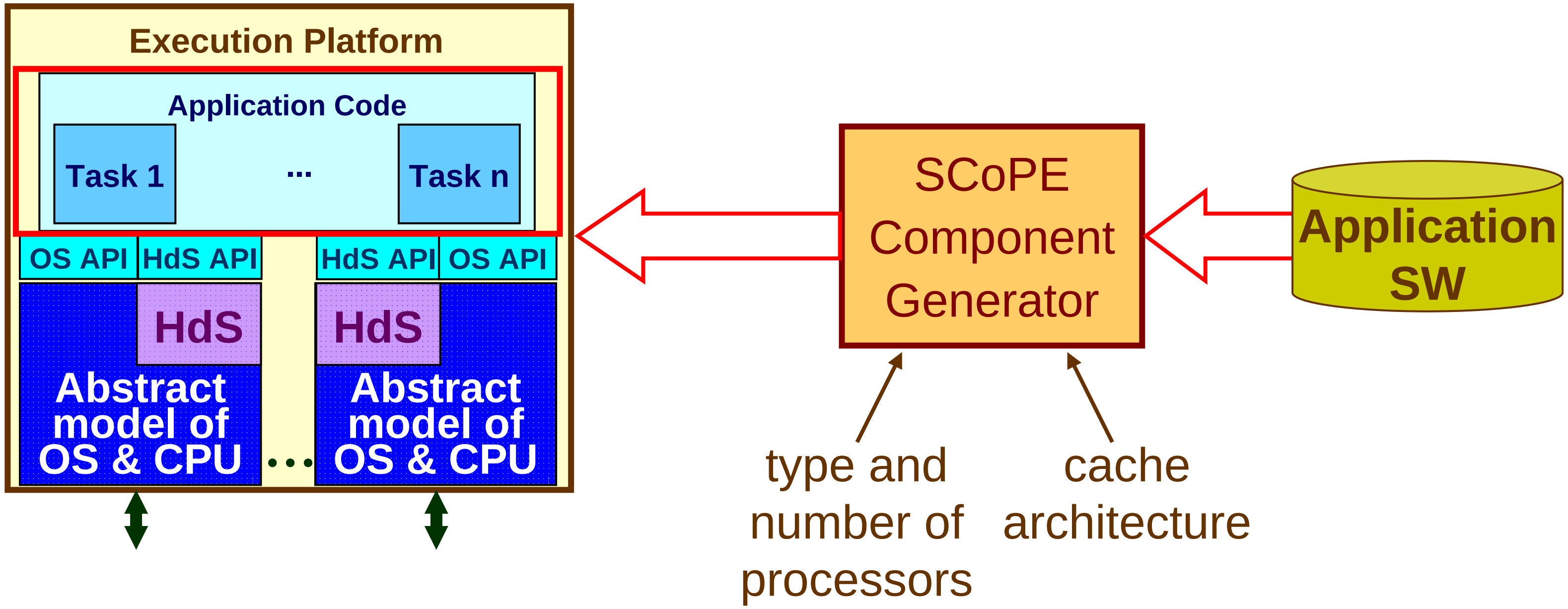


SCoPE: Improvements for Scalopes

- Data cache model
- L2 model
  - In both cases, physical addresses model needed

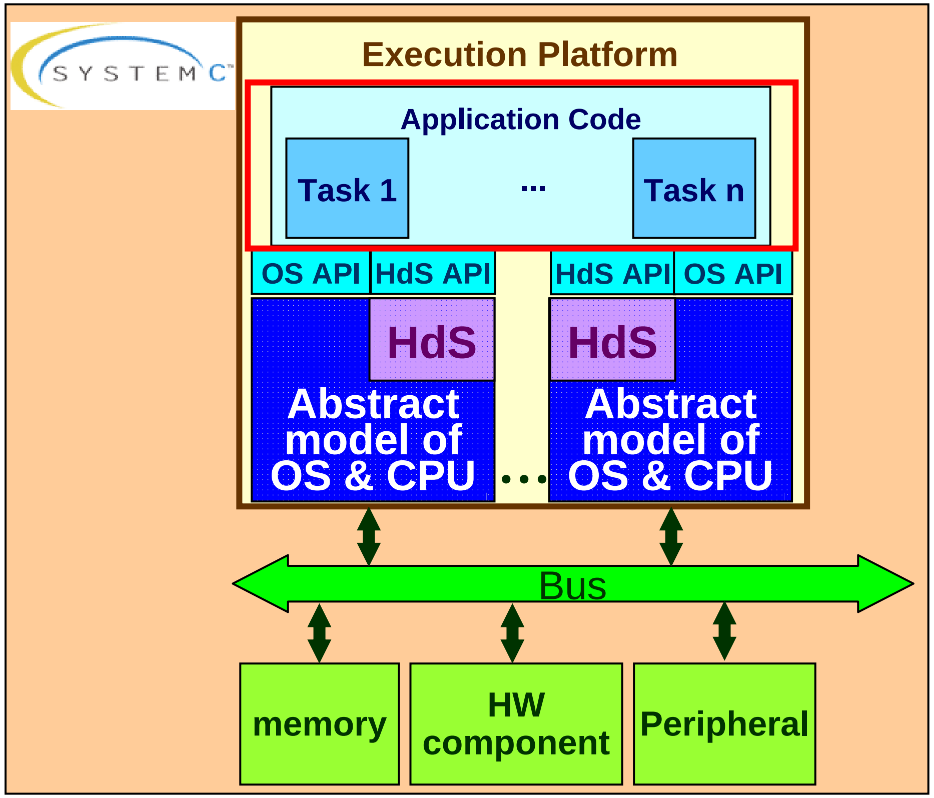
SCoPE: Improvements for Scalopes

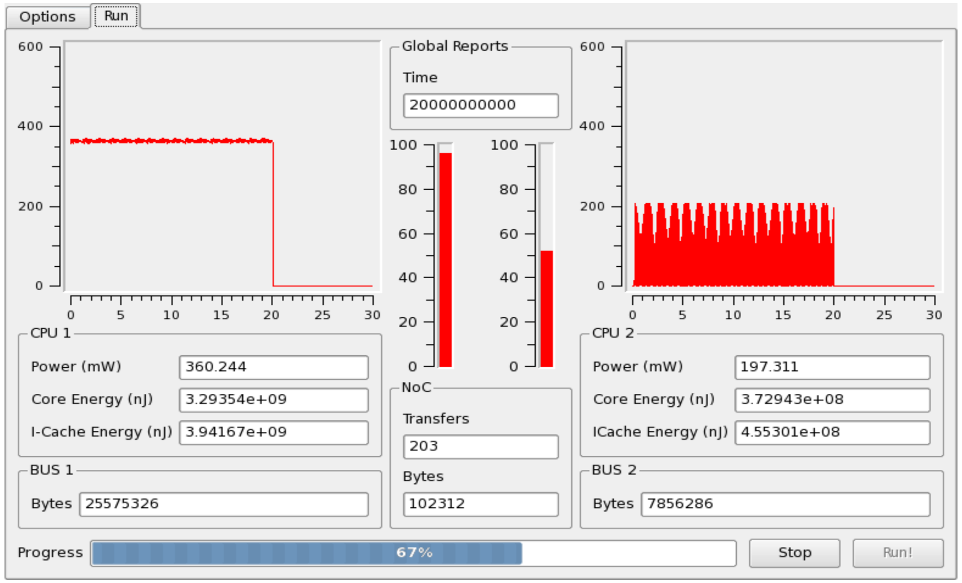
- SCoPE as a system component



SCoPE: Improvements for Scalopes

- SCoPE as a system component





Global Reports

Time: 20000000000

CPU 1

Power (mW): 360.244

Core Energy (nJ): 3.29354e+09

I-Cache Energy (nJ): 3.94167e+09

BUS 1

Bytes: 25575326

NoC

Transfers: 203

Bytes: 102312

CPU 2

Power (mW): 197.311

Core Energy (nJ): 3.72943e+08

ICache Energy (nJ): 4.55301e+08

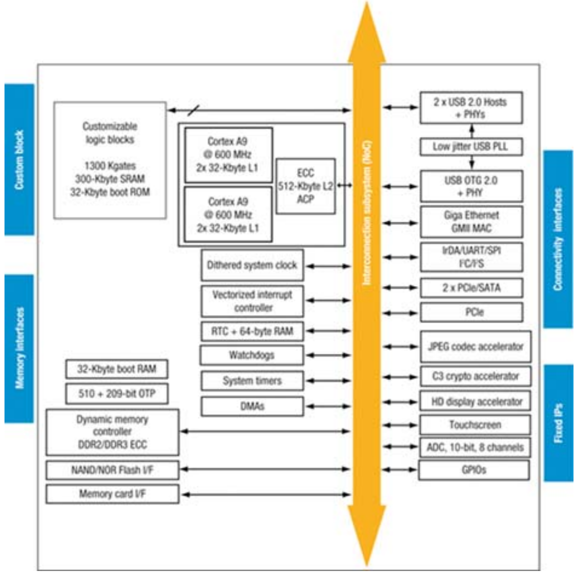
BUS 2

Bytes: 7856286

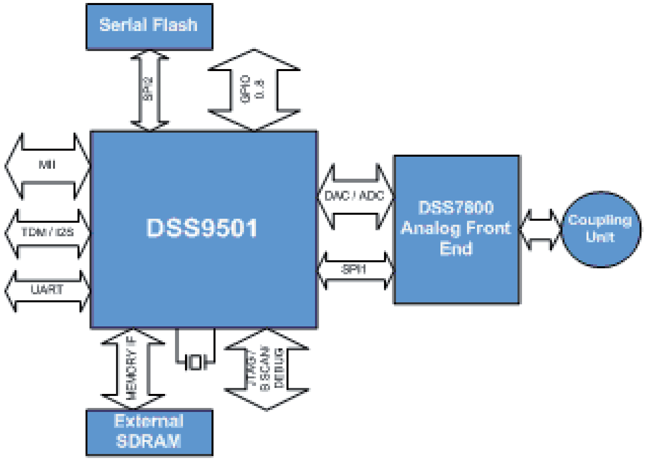
Progress: 67%

SCoPE: Improvements for Scalopes

- Spear modeling



- Power-Line Communication (PLC) modeling



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Conclusions

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Conclusions

- SW simulation
  - Essential Design Technology
  - HW/SW Embedded Systems
  - At different design steps
    - Different modeling and simulation technologies
    - Various performance*accuracy products

- SCoPE
  - SystemC Native Co-Simulation Technology
  - Specially tuned to performance analysis
    - Design-Space Exploration

Thank you for your attention

- Slides available at:
  - www.teisa.unican.es/en/publicaciones
- SCoPE available at:
  - www.teisa.unican.es/scope

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Thank you for your attention

We value your opinion and questions

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