Generation of Abstract IP/XACT Platform Descriptions from UML/MARTE for System-Level Performance Estimation

Towards a MARTE to IP/XACT Generation Framework of HW Platform Descriptions for a DSE Multilevel Performance Estimation Framework

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Goal

- Standard Format (in SW)
- Graphical, User Friendly
- Portable (Capture Tools)
- Embedded (MARTE)

- Extract Hw Platform
- Automatic
- Integration in a DSE framework
- Portable (Generation Environments)

- Standard Format (in HW)
- Traceability
- Potential Scalability
Goal

• “Abstract” Description of HW platform
  – All the component models might not be available (in the IP/XACT library)
  – Then the Generator is able to reference a generic Component
  – The Framework can generate an Executable Platform anyway
UML/MARTE related flow in COMPLEX

Configurable UML/MARTE Description

Application Mapping HW/SW platform

CFAM XML IP-XACT

SystemC (PIM)

Other COMPLEX Performance Estimation

SCoPE+ lib. + SystemC (Configurable PSM for DSE)

Performance Estimation (PE)

Fast PE DSE Tool
COMPLEX UML/MARTE Model

- Data view
- Functional view
- C&C view
- Platform view
- Architectural view
UML/MARTE Model: Architectural View

HW Instances
- + CamCtrlDev: CameraDev [1]
  - + shb_port: <Undefined> [1]
  - + ahb_port: <Undefined> [1]

+ proc_cluster: ublaze [2]
- + ahb_port: <Undefined> [1]

+ SteerCtrlDev: SteerCtrlDev...
- + apb_port: <Undefined> [1]
- + apb_slave_port: <Undefined> [1]

SW Instances
  - + raw_image_port: <Undefined> [1]
  - + position_port: <Undefined> [1]

+ CarCtrl_0: CarCtrlComp [1]
- + pos_in_road_port: <Undefined> [1]
- + steer_port: <Undefined> [1]

SW Instances
- + nrtos: xkernel.smp [1]
- + nrtos: elmax [1]

Platform

Application
SCoPE

- [www.teisa.unican.es/scope](www.teisa.unican.es/scope)

- Performance Estimation of MPSoC with NoC
  - Native Source Simulation

- Main Features
  - Output:
    - Performance Figures: Time, Power, CPU usage, Temperature,…
  - FAST:
    - Time estimation speed-up = 5 vs Virtualization / 100 vs ISS
    - Power estimation speed-up = NA vs Virtualization / 500 vs ISS
  - Input:
    - Application
    - HW/SW architecture, MPSoC with NoC
    - Output Metrics
    - IP/XACT description of HW Platform
- Functional Information: vendorExtensions
  - SPRINT (SCIPIV) context labels
    - isProcessorComponent
    - isBusComponent
    - isInternalComponent
Implementation

- Development Language: MTL / M2T

- Development Framework: Eclipse Helios
  - AcceleoMTL
  - Integrated with Papyrus MDT (UML/MARTE Specification)

- Features:
  - XML Comments for tracking Generation
  - Checks of error conditions: Dump to COMPLEX console
  - Integration as standalone plug-in and within COMPLEX plugin
Conclusions

• Tool for Automatic Generation from (COMPLEX) UML/MARTE models of generic and synthetic IP/XACT descriptions for fast DSE

• Features
  – Integrated in (COMPLEX) Eclipse DSE Environment
  – Portable to different generation environments (supporting MTL)
  – Concise and traceable IP/XACT descriptions
Future Work

• Complete IP/XACT generation

• Integration on the COMPLEX multi-level DSE framework

- Lower Level PE
- Implementation
Thanks

• For your attention

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