

PHARA()

Parallel and Heterogeneous Architectures for Real-time

ApplicatiONs

http://pharaon.di.ens.fr



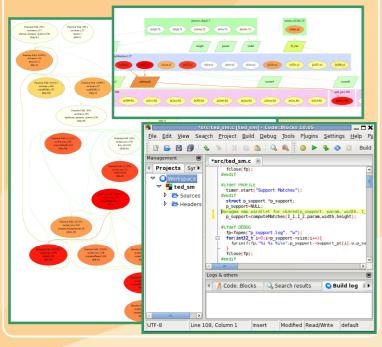
Objectives & Impact

Develop two sets of techniques and tools, aimed at exploiting low-power capabilities of embedded SoCs with heterogeneous CPU, DSP and GPU cores.

- 1. Find the most adequate software architecture taking into account hardware constraints.
 - analyze the parallel structure of an application
 - automatically generate multi-processor code.
- 2. Adapt the platform performance (e.g. frequency & voltage) to consume only the required energy.
 - run-time reconfiguration manager
 - Iow power scheduler.

Software parallelization

The legacy software to be parallelized is analyzed to identify and display (in a highly compacted form) data dependencies and opportunities for parallelization.

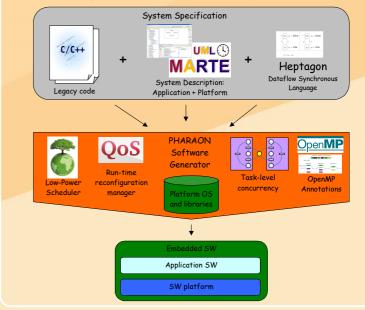


Design Flow Inputs C/C++ files Simulation Performance Performance (1)Code Generato (1) Files simulator metrics LIML/ MARTE XML files Eclipse Parallelized Parallelization (2) (2) infrastructure C/C++ files tool Performance Simulation Performance 3 (3) metrics Files simulator Code Generator Platform Physical platform Platform OpenMP (4) Source Scheduler Run-time manager (4) Binary cross-compile Files

Code Generator

The complete SW stack to be executed in each node is automatically generated from the UML/MARTE models and the functional code.

The generator produces optimized code, including additional code providing parallelism and run-time optimizations.



Demonstrators

Three demonstrators from two domains: radio and image processing, are being produced.

Two radio demonstrators:

1. MAC layer implemented on a multicore ARM based platform 2. Physical layer (L1) with real-time reconfiguration and multi- 3. stream capabilities implemented on an ARM-based platform with a specialized DSP

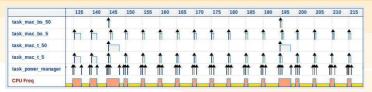
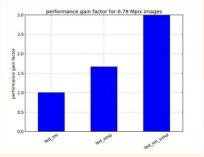


Image processing

demonstrator:

Advanced 3D stereoscopic application with real-time and high definition constraints targeting the automotive domain for human and obstacle detection



Project number 288307 / 36 Months

THALES

3.3 "New paradigms for embedded systems, monitoring and control towards complex system engineering"

imec





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Vector Fabrics

A revolutionary approach to fully automatic synthesis of embedded system software



What is eSSYN?

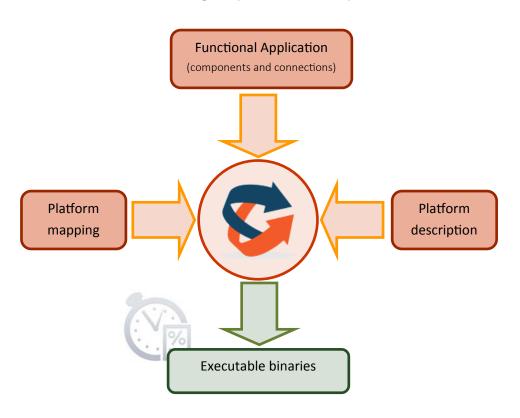
eSSYN is a software synthesis tool that automatically generates, platform specific executable binaries from a component based model of a software application and a simple model of the target hardware platform (supporting complex multicore heterogeneous platforms).

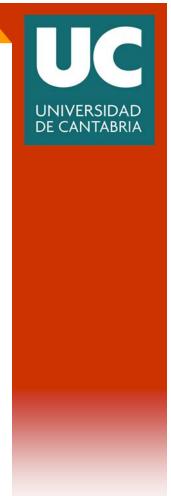
Who can benefit from eSSYN?

Anyone willing to boost the productivity of software design for embedded systems. Specially those involved in architectural design of embedded systems, including selection of target platform, mapping of software modules to available resources (GPP, DSP, GPU,...), code parallelization, application migration to new platforms, etc.

What is the main benefit of eSSYN?

eSSYN is an incredible effort saver for common system level tasks. For instance, splitting an application into two executables and mapping those to two cores of a platform can be done, from start to end (binaries) in five minutes. Doing that by hand is a matter of days.







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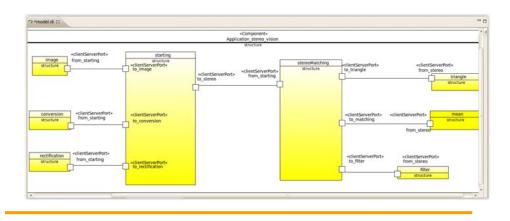
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Platform Independent Model

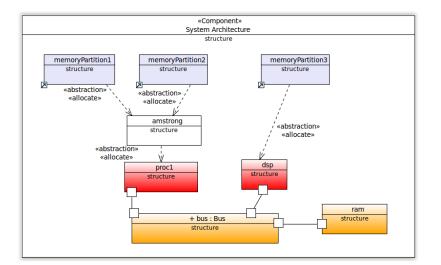
A component based model of the application is generated by the user using a simple semantic (even a wizard is available making it extremely easy to generate). This model is independent of the target HW platform and therefore is reusable among different platforms. As part of the component description, functional C, C++ or OpenCL source code is provided (actually several alternative implementations of the componet funcitionality may be included) and a description of the component interfaces. Last, a system view showing the connections among components complete the platform independent model of the application.



Platform Specific Model

eSSYN allows the user to play with different mappings of components into executables though a convenient GUI. Similarly each executable can be assigned to one of the microprocessor cores, DSP or GPU available in the hardware platform. With a simple click and drag the user can completely redefine the mapping of the application and in five minutes obtain new binaries for the new implantation, exploring this way different parallelisms, resource usages etc.

Equally powerful is the capability to map an application to different platforms in a similar way. eSSYN only needs a very simplified model for each platform to test, an upgraded System Architecture as shown below and with the click of a button a new binary is generated for the new platform.



Want to know more about eSSYN? Contact eSSYN team for a hands on demo and get to know the new way to generate complete embedded software systems in minutes.









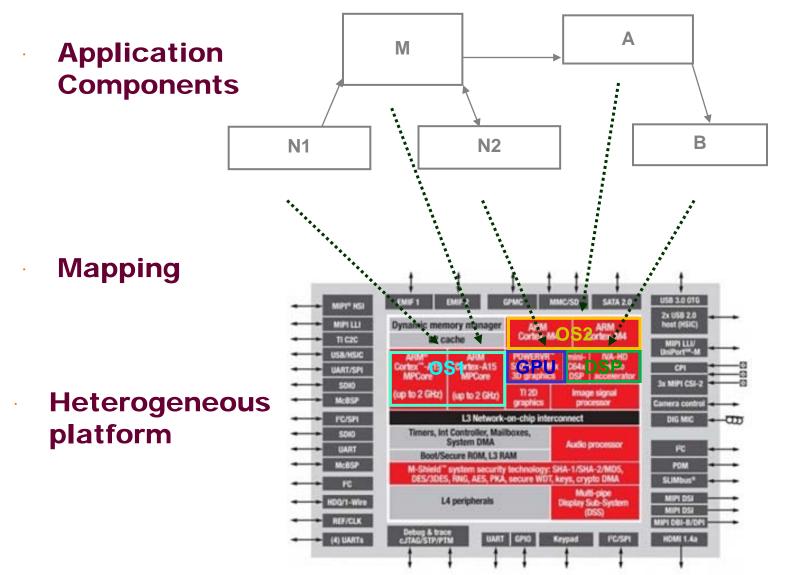
SOFTWARE SYNTHESIS FOR HETEREOGENEOUS EMBEDDED SYSTEMS

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Starting point

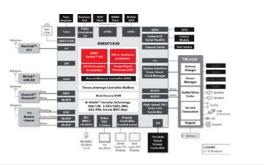
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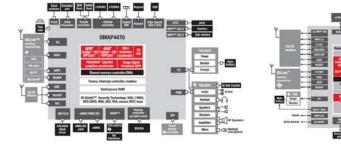


03/04/2014

Multiprocessing and heterogeneous platforms







Texas Instruments OMAP Evolution Time

Connectivity	Advanced (Connectivity	Ext Memory I/F	
FC x2	10100 Ethemet	L2 Sellch	NAND	
SPI x 4	IEEE 1508 x2		BCH 20-bit	
UARTx6	CAN x2	HS USB Phy x 2	DDRg	
Up to 124 GIPIO	-	-	mDDR	
MMC:/SD x 4		1X28 26EJ-S	LV-00R2	
Analog 12-bit ADC x 8		454MHz		
2Meps ADC x 1	16K I	32K D	128KB SFAM	
Thermal Protection	Cache	Cache	128KB ROM	
Power	Sec	User 1F		
Management	HAD	OTP AES Key	LCD Controller	
DC/DC - 4.2V	128-bit AES	SHA-2 Heating	Touchacreen	
LDO x4	Standar	Scaling		
Battery Charger	Timer x 4	PWMx8	Alpha Bending	
Audio	Watch Dog	DMA	Retation	
PS+2	System	Color Space		
SPOIF Te	ETM	JTAG	Conversion	

System Control		Connectivity			
Secure JTAB		ARM Certer ²⁴ -85			
Power Mgrit	32 KB	32 KB 32 KB 256 KB		HE MMC/ SDID x 4	
PLL + 3 Olock Reset	E-Cashe Neor	D-Cashe	L2-Ceche ETM	CSPI HS x 2/ LS x 1	
Timers	Vactor Floating Point Linit			UART + 5	
Timirs 2	2			PC+3	
FIRMA 2	Multimedia			35575 x 3	
Watch Dog	OpenGL ES	OpenGL ES 2.3 OpenVG 1.1		1-Wile	
because of the second second				Atta-6	
Memory	Hat	Hardwate Video Codecs			
ROM 32 KE		H0729 TV-Out			
RAM 128 KB				USIL HS Host x 3	
Security	lmag	Image Processing Unit			
Sahara v4	Ro	Resizing and Blending			
Trat/Zona*				Keyped	
RTIC	in the	Inversion and Rotation			
BCC v2	10	arcago Exhancement			
SHIC		Carnora			
171.023		Tringt DMA			

Freescale IMX Evolution Time

i MX 6Quad Applications Processor Block Diagram

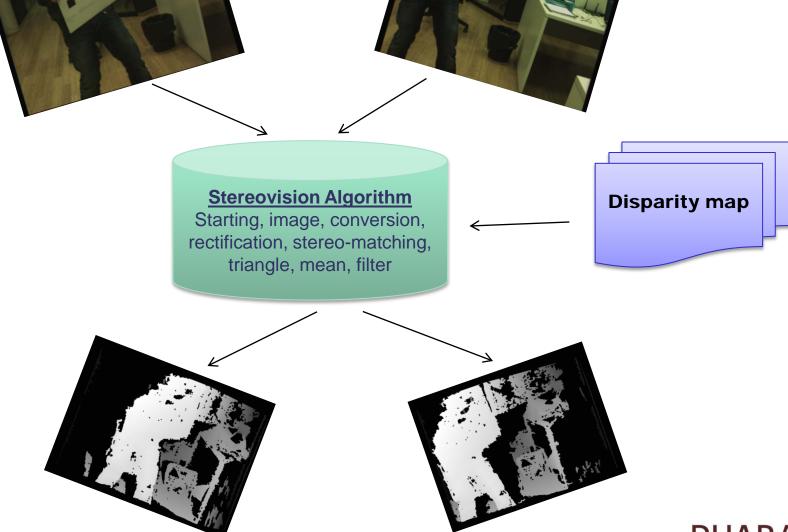
System Costrol	CPU Platern			Connectivity	
Becare JTAG		Guad ASM* Certar** AP Cera		MVC 44	USB2 HSIC
PLL ONL		SZ ND I-Gaster SZ ND D-Gaster		10 3.0 KT	Heat v3
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Smart CMA	NEON per C	NEON per Core		LIART at	SPOF
ONUX	1 MB L	1 MB L3 Cashe + VFPv3			Tayfile
Tener sll	Mattimedia			C Mispa PC x3,	PCIe 2.0 0-Lanei
PWM of	Hartware Dr	Hardware Graphics Accelerators 30 Vector Graphics			
Waluh Duy AZ	20	- 10	and a state of the	254, 19/99	FlexCAN x2 MLB150 + ETCP
Power Management	Video Codeca 1099p30 Dru/Der		Auto	12	
Power Temperature Montor	Total Concernence		AGENU .	3.9V GPIO Keypart	 IEEE* 1588
Internal Memory		Amonging Processing Unit			Library and
NM NGR	Resarg and Banding Image Enhancement Investion/Rutation			8-ATA and PHIY 3 Gops	ROHAD Critt
Geourity	-	_			LP-DORL
PND Becury Dest	Display and Camera interface HDMI and PHY 24-bit RQB, LVDB (x2)			LISED OTS	0085
natiZone Second 010	MIPLOS		20-bit CSI	LISEL HOLE	132/04, 533 MHz
Cations States	MIFI CBI2			and PHY	



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Stereovision algorithm





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Platform-independent model (PIM)

• Reusability

♦ Memory partition → Executable

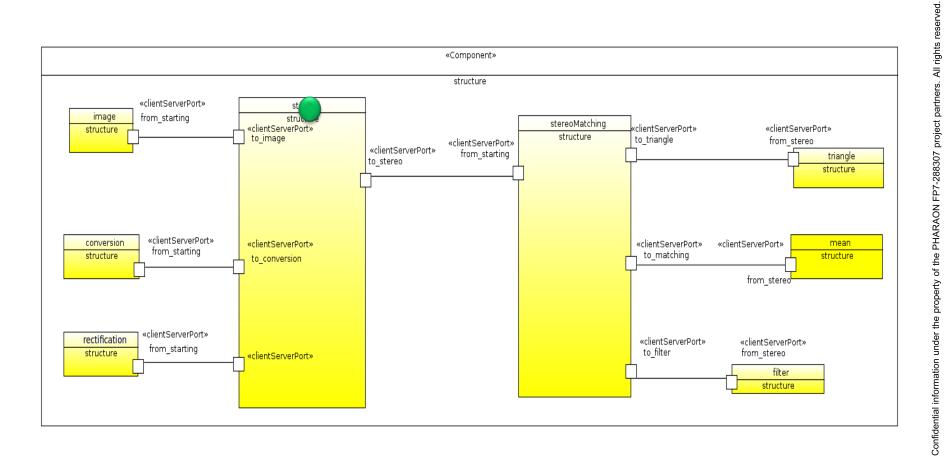
• Data protection, communications, multi-critic...

Heterogeneous platforms

• CPUs + DSP/GPU



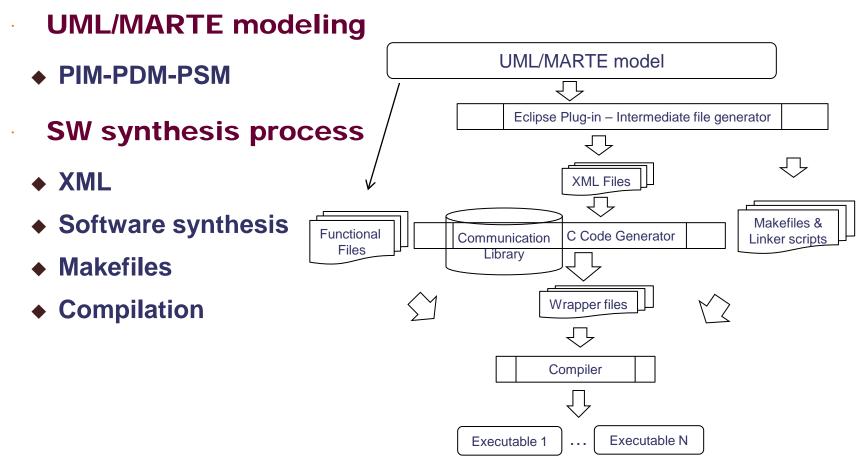
Stereovision Execution Flow





PHARAON project number FP7-288307

Tool flow





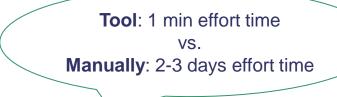
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- Project Management
- Reusability
 - Platform-independent code
- Parallelism



- Reduces in-depth knowledge of platforms
 - Reduce re-engineering effort

